

J. N. Mullan Jr.

R-216
THE 16 BY 16 METALLIC MEMORY ARRAY, MODEL 1
BERNARD WIDROWITZ

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Report R-216

THE 16 x 16 METALLIC-CORE MEMORY ARRAY,
MODEL I

by
Bernard Widrowitz

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Cambridge 39, Massachusetts

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FOREWORD

This report contains a history and some technical details of the development of our first two-dimensional, coincident-current, magnetic-core memory for binary digital computer use.

The work described herein received its impetus from the research of two men: Jay W. Forrester, who proposed the coincident-current selection scheme, and William N. Papien, who systematized the pulse-testing of magnetic cores and constructed an experimental 4-cell memory.

Signed Bernard Widrowitz
Bernard Widrowitz

Approved JW
Jay W. Forrester

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ABSTRACT

A 16 x 16 memory array of small molybdenum permalloy cores has been assembled and tested over a period of some months. Fairly reliable operation despite a rather wide dispersion of core characteristics is encouraging.

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I - INTRODUCTION

A. PRINCIPLES OF OPERATION

The operation of a coincident-current, magnetic-core memory depends fundamentally upon the "bi-stable" properties of the cores and the mechanism of coincident-current selection.²

Ferromagnetic toroids having rectangular hysteresis loops can be magnetized in either of two directions, arbitrarily called "zero" and "one". A magnetized core is a "permanent" magnet whose rectangular hysteresis properties allow it to be switched to its alternate state of flux retention only when it is excited by a magnetomotive force greater than or equal to its "coercive" force.

1. Coincident-Current Selection

If a core is excited by two windings, X and Y, the currents in each may be made small enough so that they individually provide less excitation than the "coercive" force. They may be made large enough, however, so that when applied coincidentally in time, the sum of their magnitudes is greater than the "coercive" force and switching is possible.

Many similar cores containing two windings may be arranged in a two-dimensional matrix where groups of X windings are connected in series and groups of Y windings are also connected in series. A combination of a certain X line and a certain Y line

2. Superscripts refer to similarly numbered entries in the bibliography.

identifies a core of the matrix. Thus, a single selected core in the two-dimensional system may be switched when currents are applied coincidentally to corresponding X and Y lines in such directions that the two components of magnetoactive force add algebraically to cause the desired operation. This method is not restricted to two-dimensional memories, and may be generalized for n-dimensions.¹

2. Disturbances

In the two-dimensional system described above, cores on X and Y lines common to the selected core are "disturbed" by the half-amplitude excitations if these happen to be in directions to cause switching. Disturbances reduce the amplitude of residual flux in a core. This flux reaches a steady-state value (usually 20% or 30% less than that of a freshly switched core) after many disturbances. As long as the non-selected core has a disturbing excitation which is not greater than its "coercive" force, this condition appears, rather than a relaxation toward the zero flux level.

The cores used in this memory were not bi-stable in a strict sense. That they were able to retain most of their residual flux in the face of disturbance is all that is to be implied by the expression "bi-stable". It is believed that ideal cores with perfectly rectangular hysteresis loops would actually be bi-stable.

3. Current-Selection Ratio

The larger the magnitude of the excitation delivered to the selected core, the faster that core switches; however, the greater are the disturbances, and the narrower will be the current margins for reliable use. It is desirable to switch the selected core rapidly because switching time is the most significant part of total time required to "read" or "write" at a given address (core).

In designing a coincident-current memory, one always wishes to impart the most excitation with the least disturbances. The ratio of the excitation of the selected core to the greatest disturbing magnitude is called the selection ratio.

The selection ratio is a function of the configuration and connections of the driving lines of the memory. It has a value of 2 for the two-dimensional system described above. If the total ($X+Y$) excitation of the selected core is called I_m , the disturbing excitations are $\frac{1}{2}I_m$ in magnitude. Another two-dimensional system may be obtained by placing a Z winding on each core in addition to the X and Y. All of these Z windings must be in series. The selected X and Y lines then draw $\frac{2}{3}I_m$, while $-\frac{1}{3}I_m$ is applied to the Z line. The selected core receives I_m , and the disturbing excitations are either plus or minus $\frac{1}{3}I_m$ depending on whether or not the disturbed core is on a selected X or Y line. The selection ratio is therefore 3, the "best possible" two-dimensional current-selection ratio.¹

4. Sensing (Read-out)

As we have seen, it is possible to set any core in the two-dimensional system in either direction (i. e., to write a "zero" or a "one"). To read out the information stored, we have only to write a "zero" into the selected core. If a "zero" is already stored, no switching occurs; if a "one" is stored, switching takes place. A sensing winding, threaded through every core in the system, is able to pick up an induced voltage if any core switches, so that it is possible to determine the state of the selected core prior to the reading operation.

Reading is destructive and clears the memory core. If it is necessary to retain the information in a core for further reading, provision must be made for re-writing after each read-out.

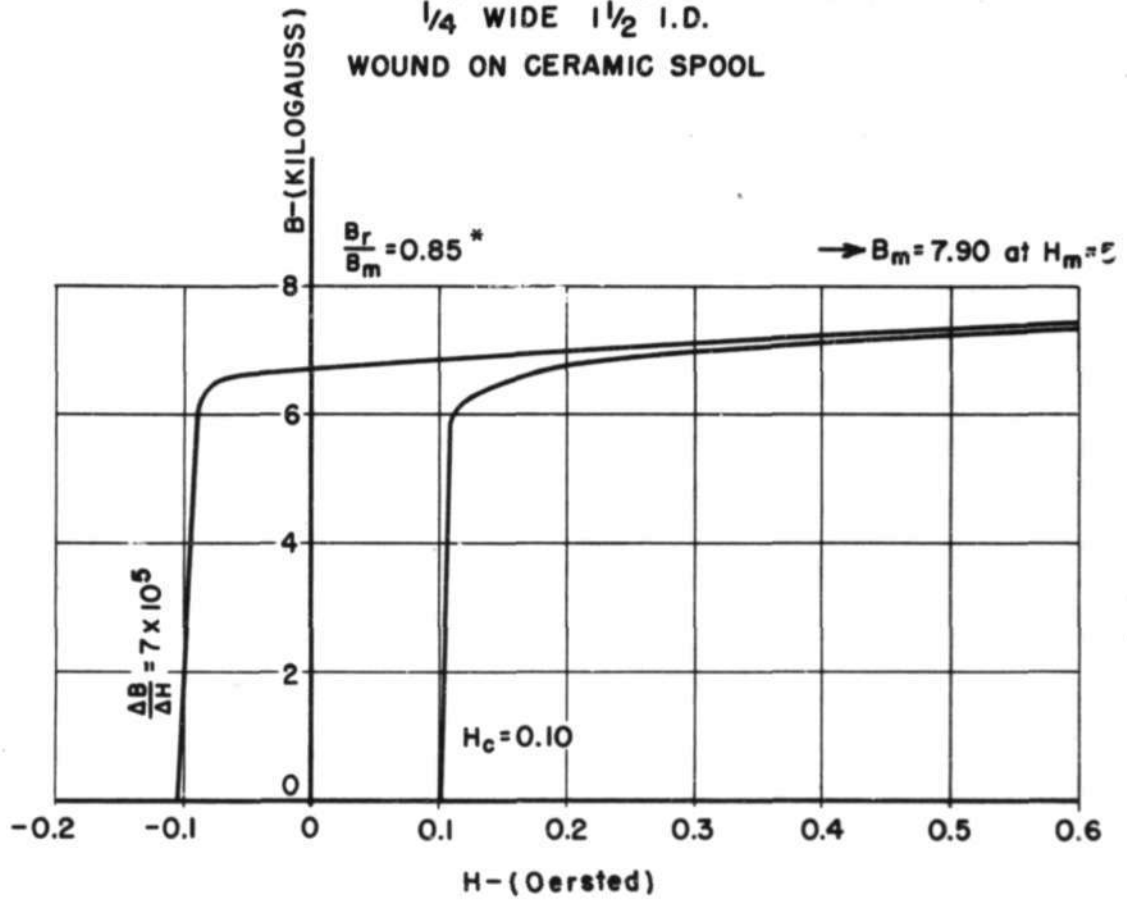
B. WINDINGS AND CORES

At the outset, it was decided that the cores were to have straight-line, single-turn windings, driven by vacuum tubes. The sensing winding was also to be single-turn.

The cores to be used were made of molybdenum permalloy, 1/4 mil thick tape, 1/8" wide, wound 5 wraps deep on a ceramic bobbin so that the diameter of the path of the metal is 3/16". These cores were fabricated by Magnetics, Inc. The d-c saturation hysteresis loop for a core of this type of material is shown in Figure 1.

D-C HYSTERESIS LOOP
CORE NO. 216

79-4 PERMALLOY
0.26 MILS
1/4" WIDE 1 1/2" I.D.
WOUND ON CERAMIC SPOOL



* $B_r/B_m = 0.915$ for $B_m = 7.45$

CURVE NO. 5112
ARMCO RESEARCH LABORATORIES
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FIG. 1

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II - CORE TESTING

Considerable variation in properties was found to exist among the cores. Since these cores would be excited by common driving lines in a coincident-current memory, and would have their flux paths linking a single sensing or pickup winding, it was quite important to select those cores whose characteristics clustered as closely as possible.

Standards of comparison were established to check each core for switching speed and voltage generated in a single turn, when switched under an excitation of I_m . The single-core pulse tester (described in reference 4) was used exclusively in the acceptance testing. The waveforms of the voltages induced by the cores when driven by identical currents on the pulse tester allow grading with respect to the above characteristics. From the 500 cores available, 256 cores were to be selected. It was desirable to maintain a history of each core. To facilitate this, the cores were color coded.

After testing 50 of the cores, W. Papian selected two cores, numbers 1 and 9, as standards whose properties would most likely bound those of the final 256.

The single-core pulse tester was set to simulate memory operation with a 2-to-1 selection ratio in current. Driving currents were optimized (when averaged over cores 1 and 9, best

combination of one-to-zero amplitude ratio, switching speed, and ability to withstand non-selecting disturbances). The waveforms of cores 1 and 9 were grease-penciled on the scope face, and the regions were labeled as shown in Figure 2.

The following production testing procedure was initiated: a jig was made that could accommodate a string of 10 cores in addition to the standards 1 and 9. This jig was plugged into the single-core pulse tester (Figure 3). A small pickup loop was threaded through a core and clipped onto the scope input. The scope and pulse tester were checked with each group of 10 cores by comparisons of the outputs of cores 1 and 9 against the grease-pencil curves on the scope. A single quantity could describe a core for acceptance consideration. As found by experiment, all cores having the same amplitude of voltage output per turn at some time after being excited (see vertical grease-pencil lines on Figure 2) were fairly similar with respect to their other critical properties.

The results of the pulse test are given in Figure 4. The distribution was not smooth because the widths of the grading regions were not identical. Also the positions of the grading boundaries were judged visually. The largest ratio of switching outputs of any two accepted cores was about 1.6 to 1.

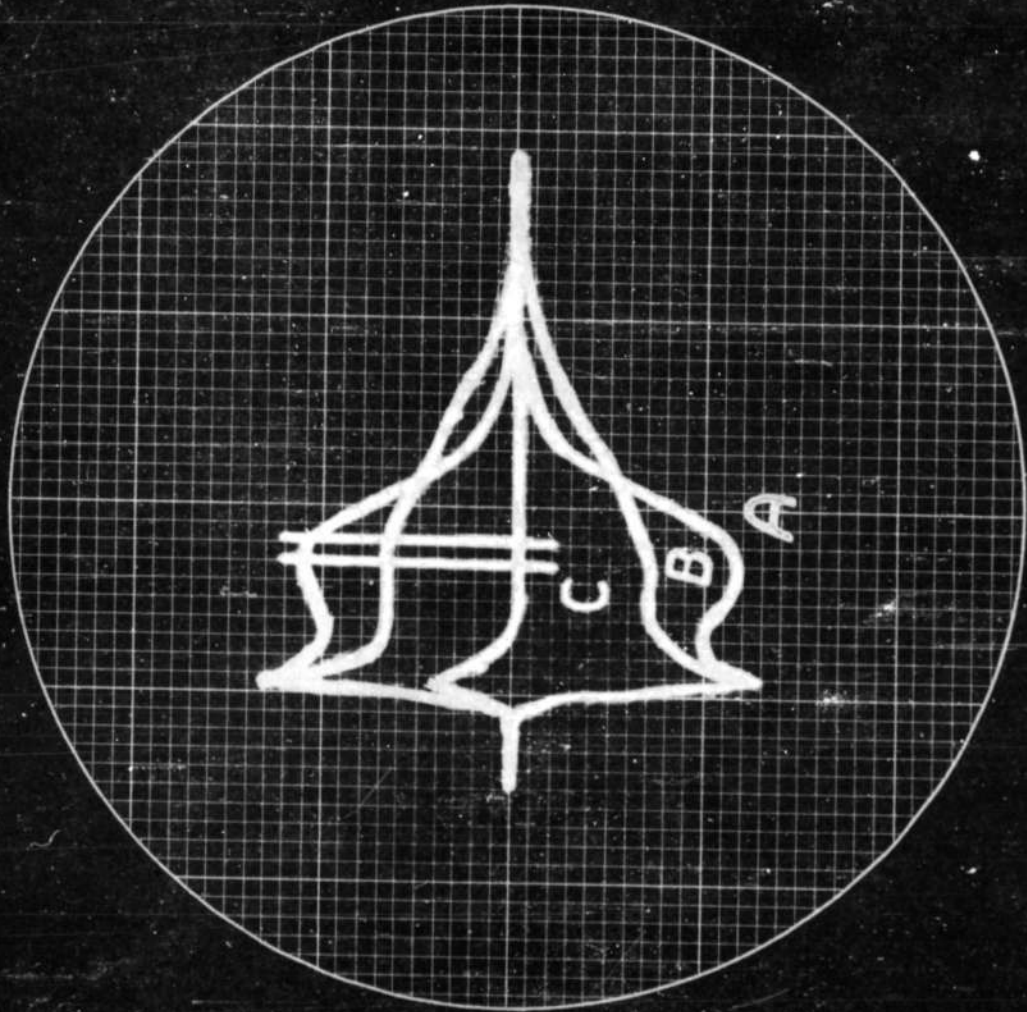


FIG. 2
PULSE TEST TEMPLATE

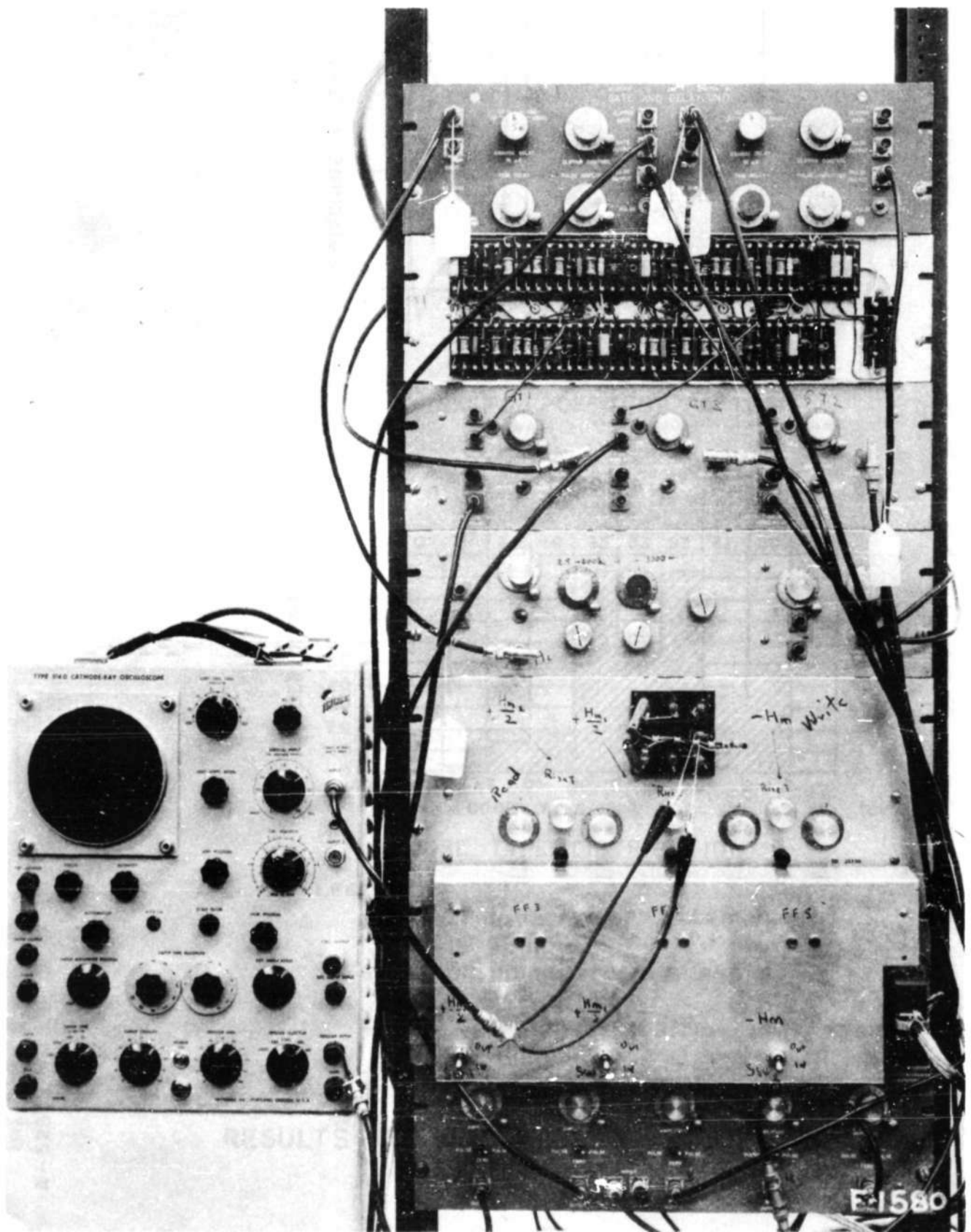
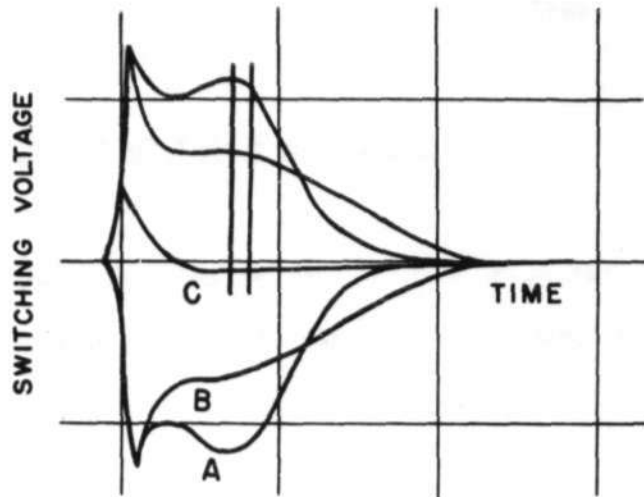
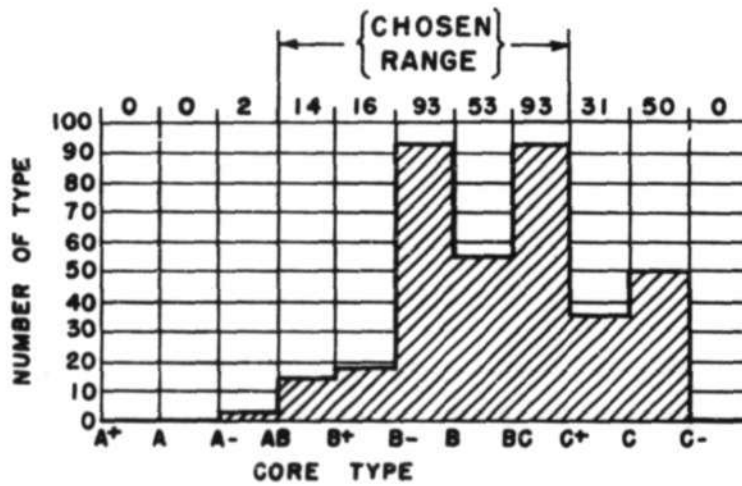


FIG. 3
SINGLE-CORE PULSE TESTER AND
JIG FOR PRODUCTION CORE TESTING

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A SKETCH OF TEST PATTERN



CORE TYPE DISTRIBUTION

LEGEND:

- AB: IF ON BOUNDARY OF A AND B
- B: IF IN REGION B
- BC: IF ON BOUNDARY OF B AND C
- C: IF IN REGION C
- + AND - INDICATE POSITION IN A REGION

FIG. 4

RESULTS OF SINGLE-CORE PULSE-TESTING

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III - DESIGN OF THE 16 x 16 ARRAY

After 256 cores were selected, the next step was to design and build the memory array. An array is a mesh of driving lines arranged so that it provides a supporting matrix for the memory cores.

The array was designed to have 16 X addresses, 16 Y addresses, and one Z address. The driving-current sources were able to draw current only in a single direction; and, because it was necessary to provide for core driving in both directions, two sets of X, Y, and Z lines were planned. A sensing winding was to be threaded through every core in the array in addition to the above; thus, a total of seven lines were concurrent at each core.

A 4 x 4 model of the wiring is shown in Figure 5. The X and Y coordinates were chosen arbitrarily. Current flowing from left to right was called "read", or "write 0", while current from right to left was called "write 1".

There were two reasons for a diamond rather than a square matrix. First, the ratio of inside diameter to length of bore of a core was such that it was impossible to pass two straight mutually perpendicular lines through it. Second, the diamond shape allowed short lead connections to the X drivers above and the Y drivers below the array.

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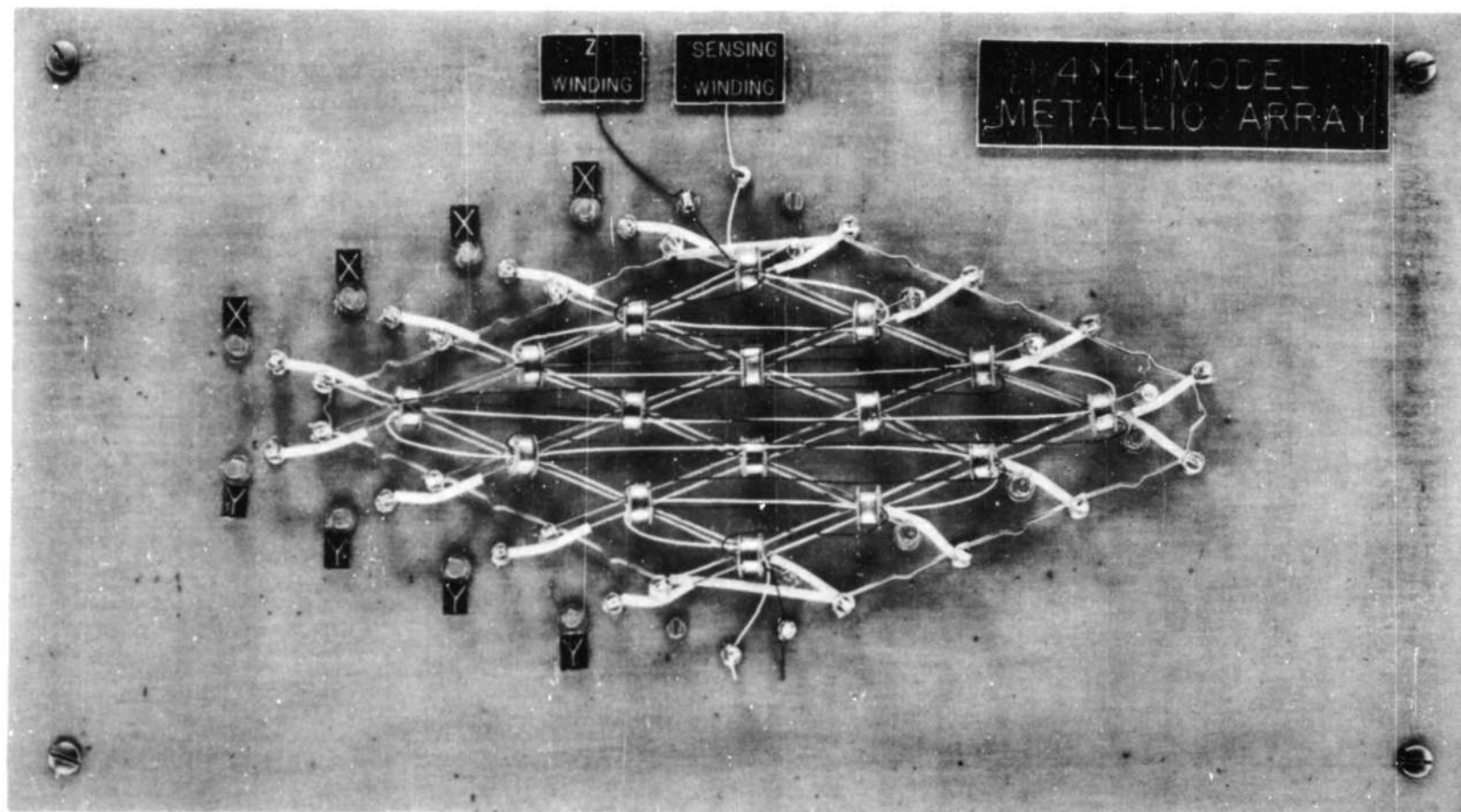


FIG. 5

4x4 MODEL OF THE METALLIC CORE ARRAY

F-1581

The sensing winding was drawn through every other core (along any X or Y line) in the same direction. This was quite different from the Z-dimension "write-1" line, which goes through every core from left to right in the positive sense. The sensing winding and only one Z-dimension winding are shown for clarity and contrast. The sensing winding was designed so that read-out pulses from non-selected cores (noise) would cancel. A discussion of this effect in a 4-core memory may be found in Engineering Note E-406.⁵ A consequence of the weaving of the sensing winding is that the sensing amplifier had to be made to operate on positive-going and negative-going memory output pulses without discrimination.

The array was built on a piece of phenolic board to fit a standard 19" rack; a photograph is shown in Figure 6.

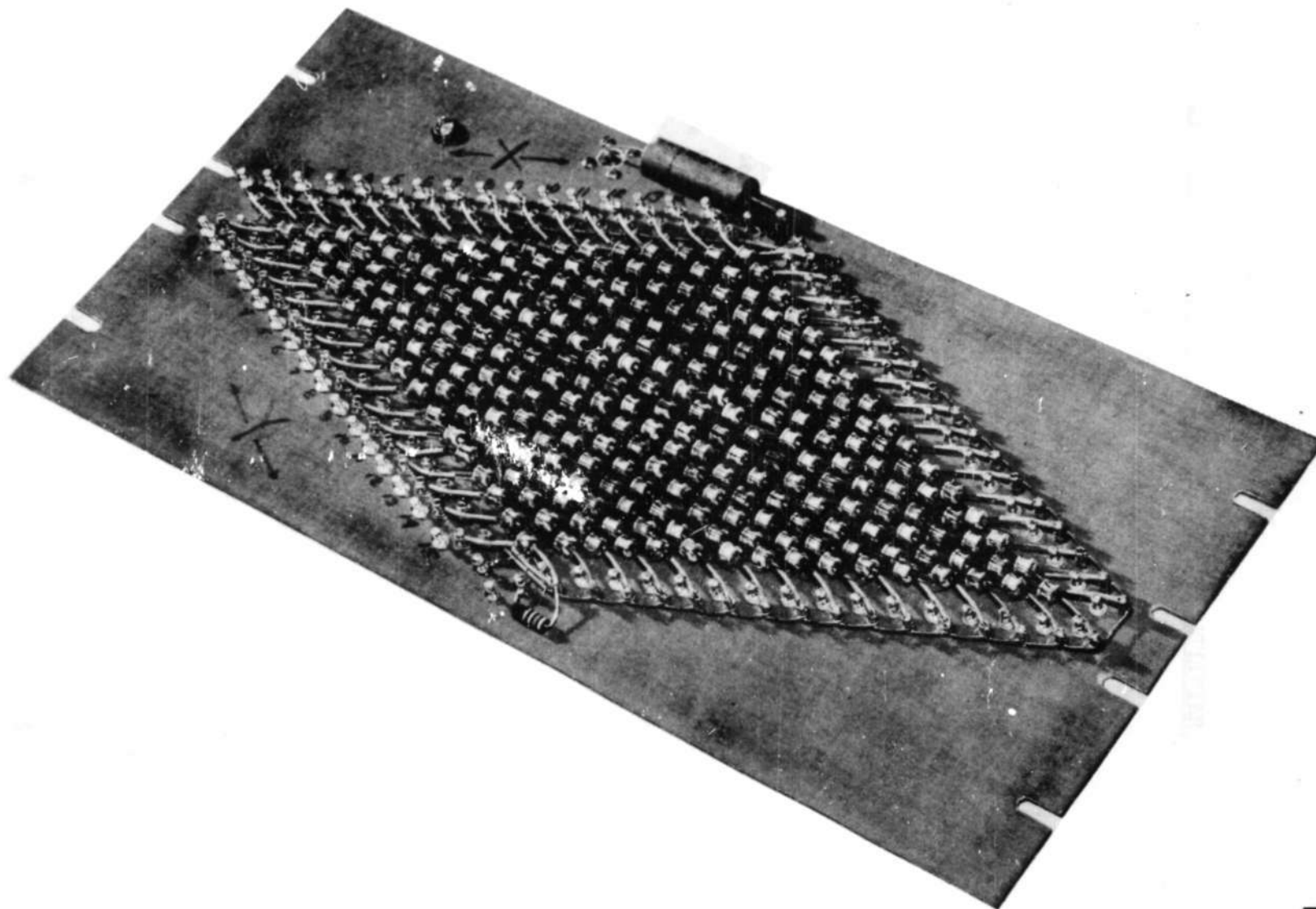


FIG. 6
THE 16 x 16 METALLIC CORE ARRAY

IV - ADDRESS SELECTOR, DRIVERS, SENSING AMPLIFIER,
AND ASSOCIATED ELECTRONICS

Two types of electronic units were used in the operation of the 16 x 16 memory: special "breadboard" panels, and standard M. I. T. and Burroughs pulse test equipment.

The pieces of standard test equipment may be thought of as logical "black boxes" that trigger the "breadboard" units by supplying pulses and gates in certain time sequences and are discussed in Chapter V, BLOCK DIAGRAMS.

The "breadboard" panels, which include the vacuum-tube line drivers, the flip-flop address selectors and associated crystal matrices, and the sensing amplifier, actually perform the work of running the memory. Because these units are peculiar to an electronically driven magnetic-core memory, they are of interest and will be discussed.

A. ADDRESS SELECTION AND DISPLAY SCOPE

The problem of address selection in a 16 x 16 memory is that of current-pulsing one X line of 16 and one Y line of 16. The problem was solved by energizing the driving tubes in tandem and biasing off the non-selected ones.

In computer use, a binary address would be pulsed into the memory before a "read" or "write" order. The address would be stored in the X and Y flip-flop address selectors at least

until the subsequently ordered operations were completed. These flip-flops supply the biasing information by operating the X and Y crystal matrices, whose output lines are connected to the control grids of the line-driving tubes.

The address flip-flops used were the 6Y6 type (Fig. 7). Each of the two banks of 4 (X and Y) was designed to work directly into a 16-position crystal matrix (Fig. 8) which was actually part of the plate loads of the flip-flops. A crystal matrix input line presented 630 ohms to ground to the corresponding flip-flop plate circuit. The selected output bias line of each coordinate was at ground potential; all other matrix outputs were 30 volts below ground.

A simple systematic way of indexing addresses was used in testing the memory. The X and Y address flip-flops were connected to count. The X set counted one for every pulse of a clock, while the X end carry was used to trigger the count input of the Y flip-flop bank. Thus the cores in the array could be repeatedly "scanned" in the manner of a conventional television system. Decoders were attached to each flip-flop set, so that X and Y analog voltages were available which were proportional to the binary numbers stored in the X address flip-flops and Y address flip-flops respectively. These voltages were applied to the horizontal and vertical inputs of a display oscilloscope. Because the address flip-flops remain in a steady-state during the "read

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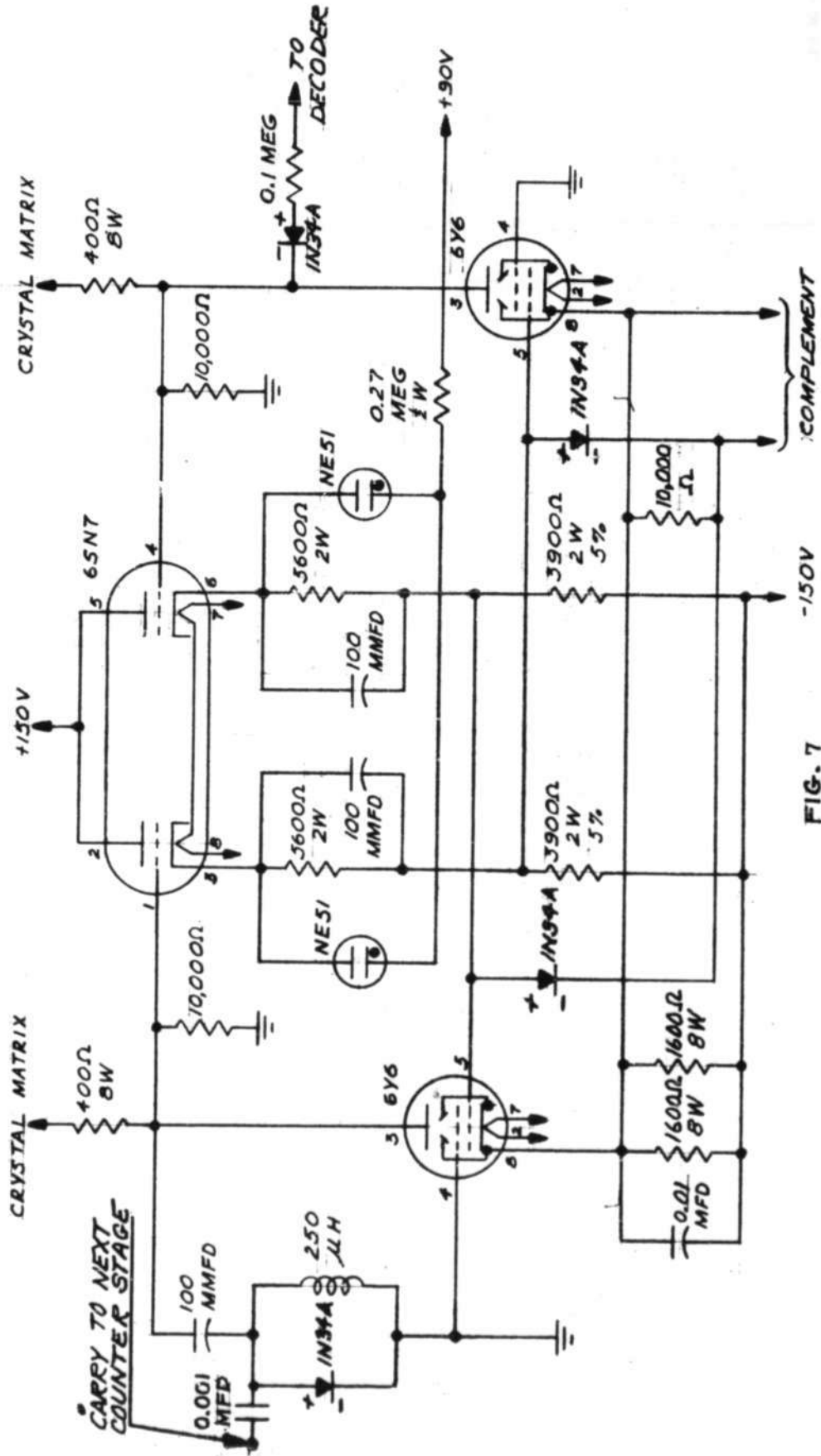
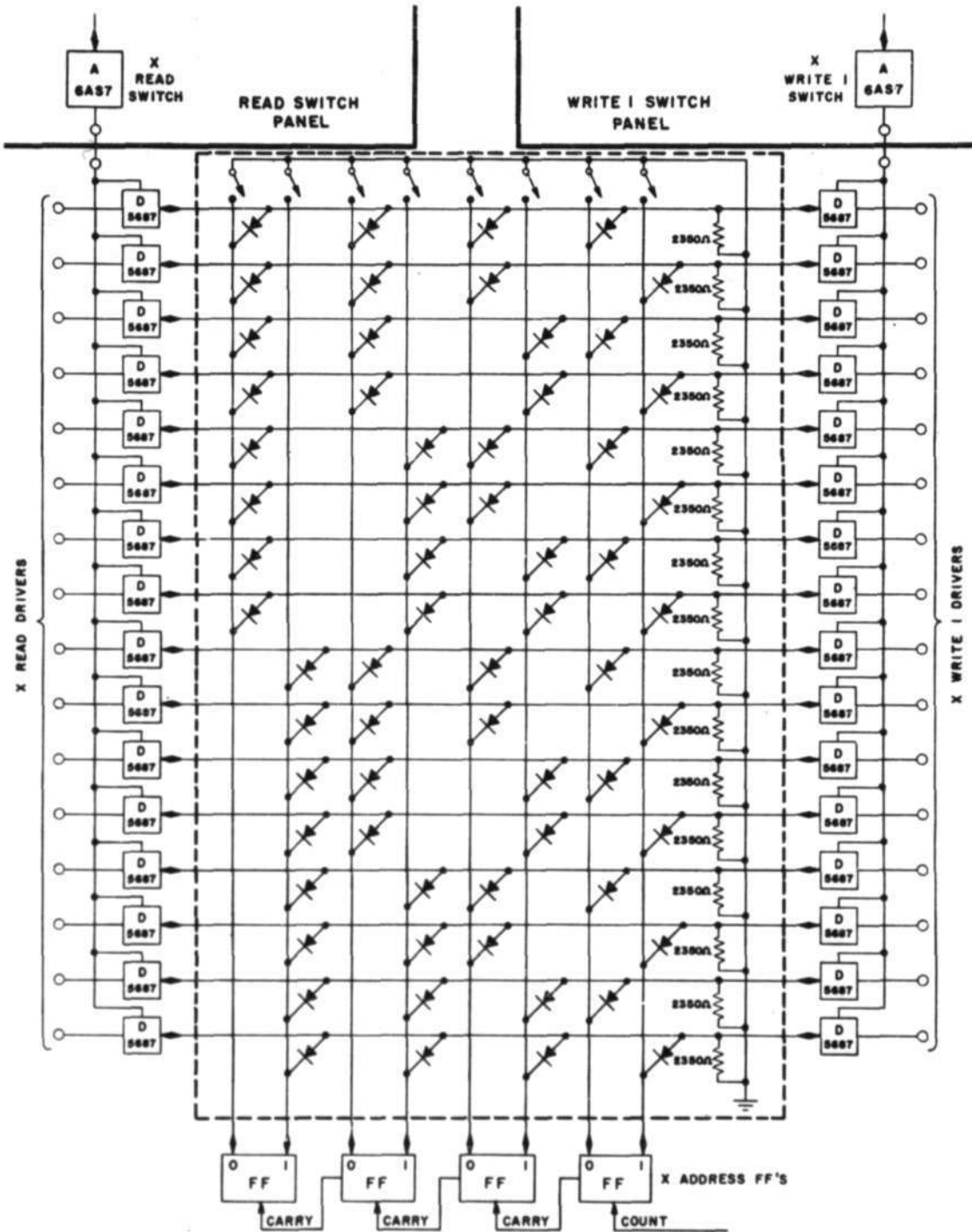


FIG. 7
CIRCUIT SCHEMATIC
ADDRESS SELECTION FLIP-FLOP



NOTES:
 1. Y CRYSTAL MATRIX IDENTICAL
 2. ALL DIODES ARE 1N34'S

FIG. 8

FUNCTIONAL SCHEMATIC
 METALLIC ARRAY X CRYSTAL MATRIX
 AND X DRIVER PANEL

and "write 1" operations, time is available to intensify the display scope if a ONE is read out of a given core. Every address in the array has a corresponding position on the display scope so it is possible to display the information content of the memory as a set of blanks and bright spots as long as the array is scanned rapidly enough to prevent flicker.

B. DRIVERS

The drivers, or the current sources which energize the array, may be divided into two symmetric groups: those used to "write 0" or "read" and those used to "write 1". Each of these groups contains a set of 16 X drivers, 16 Y drivers, and one Z driver. The circuit used (Fig. 9) was designed by Kenneth Olsen.

Each set of drivers, the "X-read" drivers for example, consisted of a group of cathode followers (5687's) all having a common cathode resistor returned to -150 volts. The control grids were connected to the X-crystal matrix ds mentioned above. Each plate was connected to its proper X-read driving line on the array, thence to +250 volts. The fact that all the cathodes were connected together allowed the cathode bias developed by the conducting tube to help the crystal matrix cut off the non-selected drivers. Normally, the cathodes' potential, held up by a 6AS7, allowed no current to flow in any of the driving lines, including the selected line. When it was desirable to apply a pulse of current, the proper 6AS7 was cut off and the selected driver then drew current. The 6AS7's associated electronics were mounted on separate

panels called "switch panels" (Fig. 10). These panels, "X, Y, Z read", and "X, Y, Z write 1" were responsible for switching on the selected drivers at the proper times. They, in turn, were controlled by the gate outputs of gate and delay units.

C. SENSING AMPLIFIER

The last "breadboard" panel to be considered is the sensing amplifier. This device was designed to produce 50-volt, positive-going gates from the positive and negative* input gates with amplitudes ranging from 5 to 35 millivolts induced in the sensing winding by the selected core. The output of this unit was to be used to control the suppressor grid of a gate tube. The input signals had rise and fall times that ranged from $\frac{1}{2}$ microsecond to 3 microseconds and lasted from 5 microseconds to 15 microseconds. The PRF could be random.

A schematic of the sensing amplifier is shown in Fig. 11. It consists of 3 stages of a-c-coupled linear amplification; a phase inverter, and two cathode followers providing output across a common cathode resistor.

The first 3 linear stages had a maximum gain well over 15,000. The remainder of the amplifier had a gain of about 0.8. The cathode followers in the output stage were biased almost to cutoff, and the grids were fed signals 180° apart from the preceding phase

* Refer to Chapter II for a description of the sensing winding.

inverter. When either grid went positive, the corresponding tube conducted as the other was cut off. Therefore, the output was always a low-impedance, positive-going signal proportional to the absolute value of the input.

The lower level of the output was clamped to a variable bias supply. Since discrimination between ZEROS and ONES was to be made on an amplitude basis in a gate tube, it was necessary to adjust this bias so that the ZEROS were below the threshold when the ONES were well above this threshold. The size of discrimination was determined by the incidence of the scanning pulse (0.1 microseconds) applied to the control grid of the gate tube. This function will be discussed further in Chapter V.

D. PHOTOGRAPHS OF BREADBOARDS

Fig. 12 shows the X-read and write I drivers and the array of cores. Fig. 13 shows the reverse side of the array and the X drivers. (Note coax cable leading from sensing winding to sensing amplifier.) Fig. 14 shows the entire system.

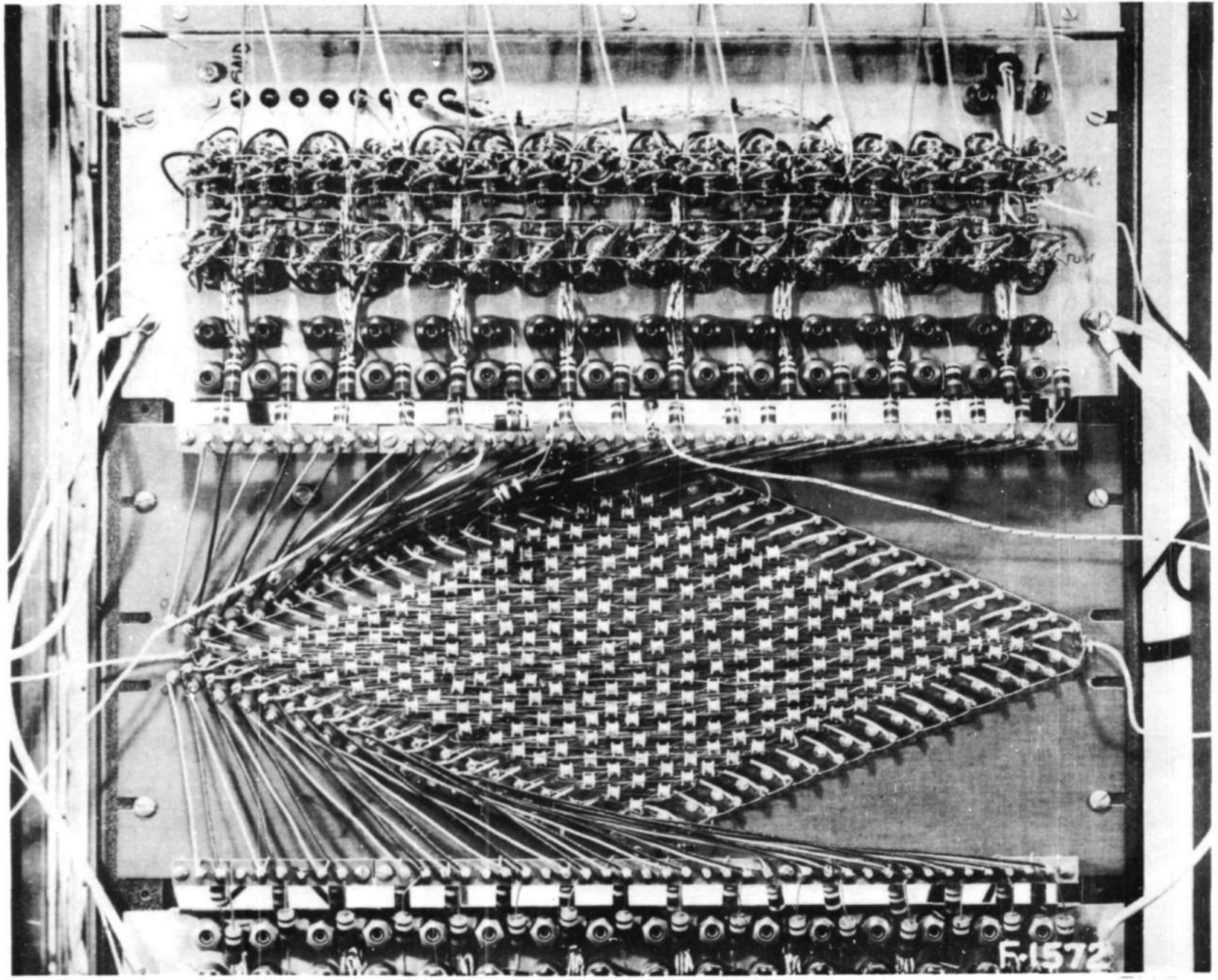


FIG. 12
16 X 16 METALLIC CORE ARRAY AND THE "X" READ AND WRITE 1 DRIVERS

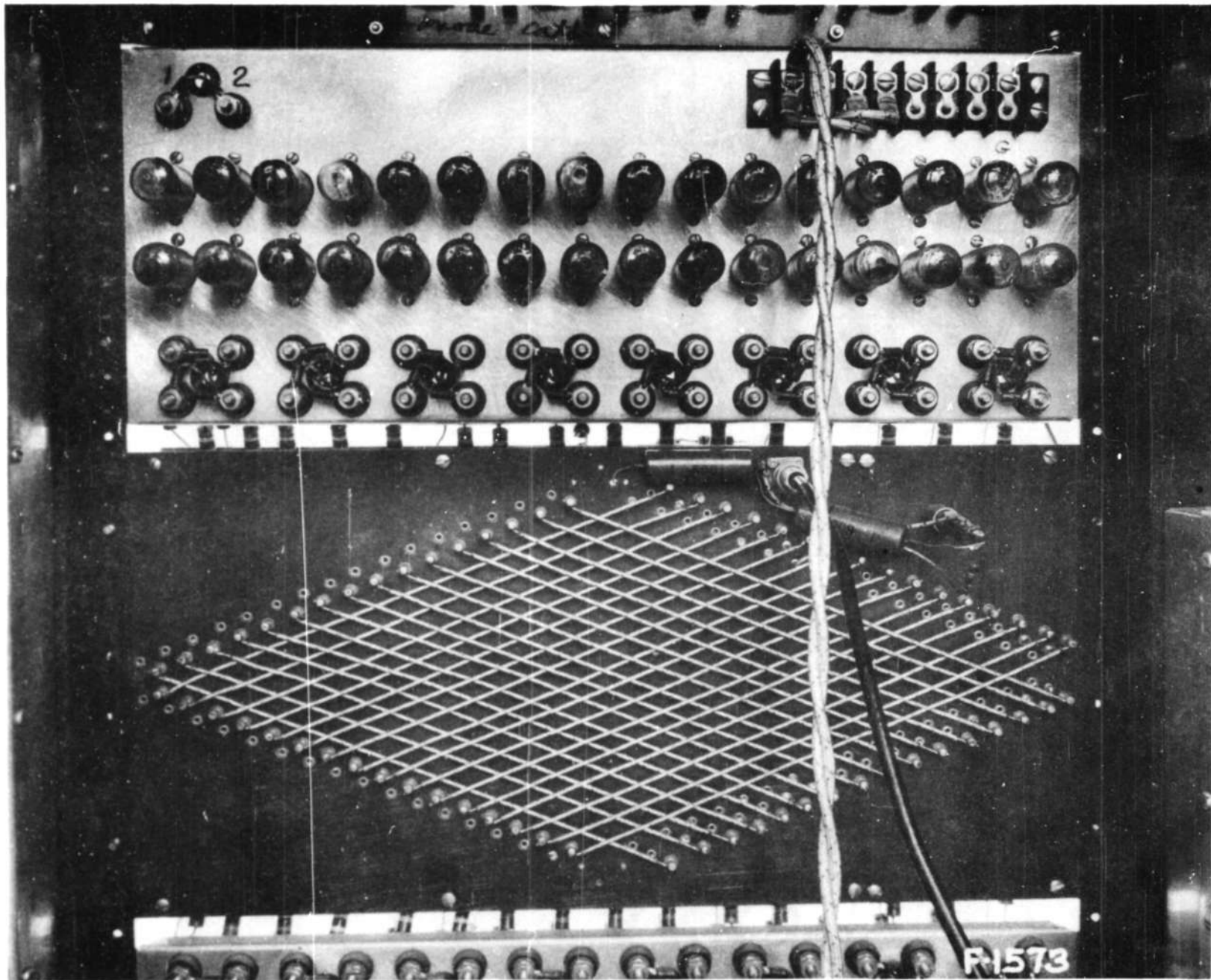


FIG. 13

REVERSE SIDE OF 16 X 16 METALLIC CORE ARRAY AND THE "X" DRIVERS

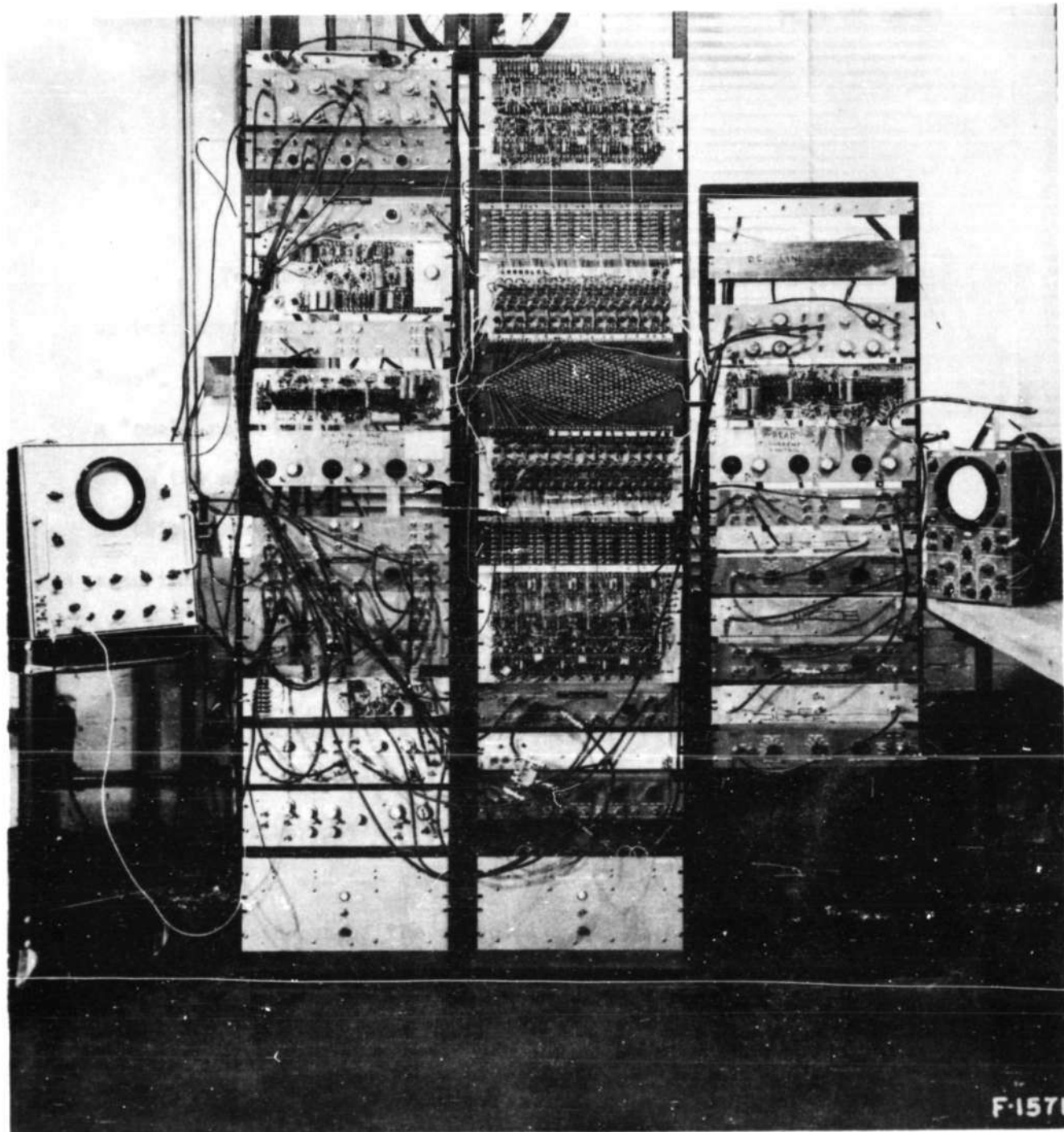


FIG. 14

16x16 METALLIC CORE MEMORY AND
ASSOCIATED TEST EQUIPMENT

A-52348

V - BLOCK DIAGRAMS

To simulate memory action, a logical system was set up to: approach a core and ask if it contains a "zero" or a "one". If it contains a "zero", leave it alone. If it contains a "one", re-write that "one" (it was destroyed by the asking). Go to the next core and repeat these operations. A block diagram of this system, utilizing standard test equipment units, may be seen in Fig. 15. The gate and delay units are adjusted to follow the timing diagram of Fig. 15. The clock pulse initiates the "read" gate by triggering gate and delay (G&D)#1 and clears a one-bit buffer storage flip-flop #1. During that gate, G&D #3 pulses the control grid of Gate Tube (GT) #2, the sensing gate tube. The buffer storage is either set or remains on "zero" after the sense pulse. This depends on whether the sensing amplifier has a large signal (ONE being read out of the selected core) or a small brief signal (ZERO being read out of the selected core, the selection being determined by the address that the X and Y flip-flops happen to be set on at the time). At the end of the read gate, G&D #1 pulses GT #1. A pulse is emitted by GT #1 to trigger G&D #2 (initiate the write 1 gate) only if buffer storage was on the "one" position (i.e., only if a ONE was read out of the selected core). Time is allowed for the complete read, re-write cycle before G&D #4 sends out a count pulse

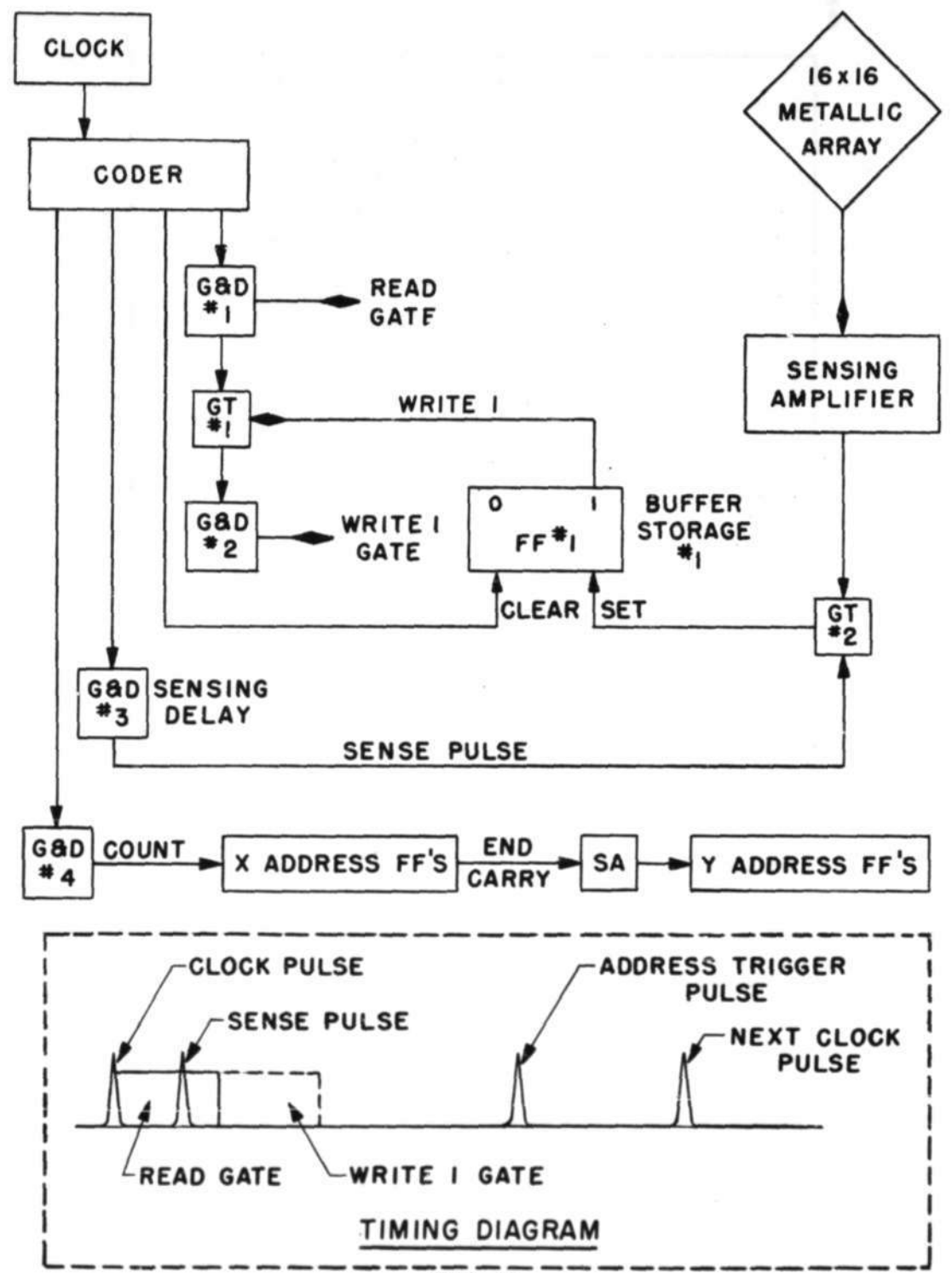


FIG. 15
BLOCK DIAGRAM

BASIC TEST SYSTEM OF MAGNETIC MEMORY

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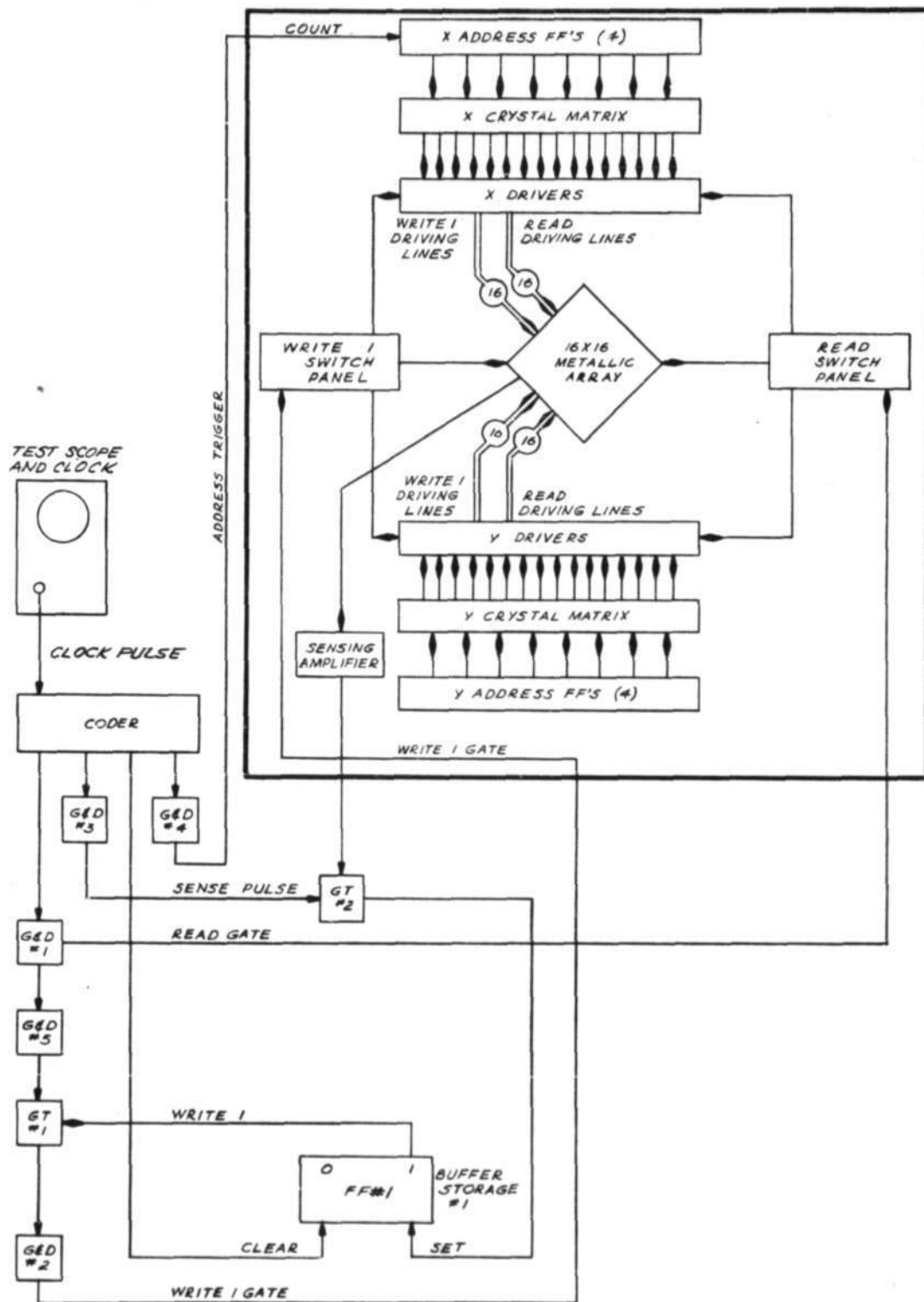


FIG. 16
 BLOCK DIAGRAM, BASIC TEST SYSTEM OF MAGNETIC MEMORY
 SHOWING CONNECTIONS OF DRIVERS AND ADDRESS SELECTORS

(address trigger) to set the X and Y address flip-flops to the next address. This is done before the next clock pulse, so that the driver grid biasing potentials will be applied for the next reading, re-writing operation.

A. THE BASIC BLOCK DIAGRAM

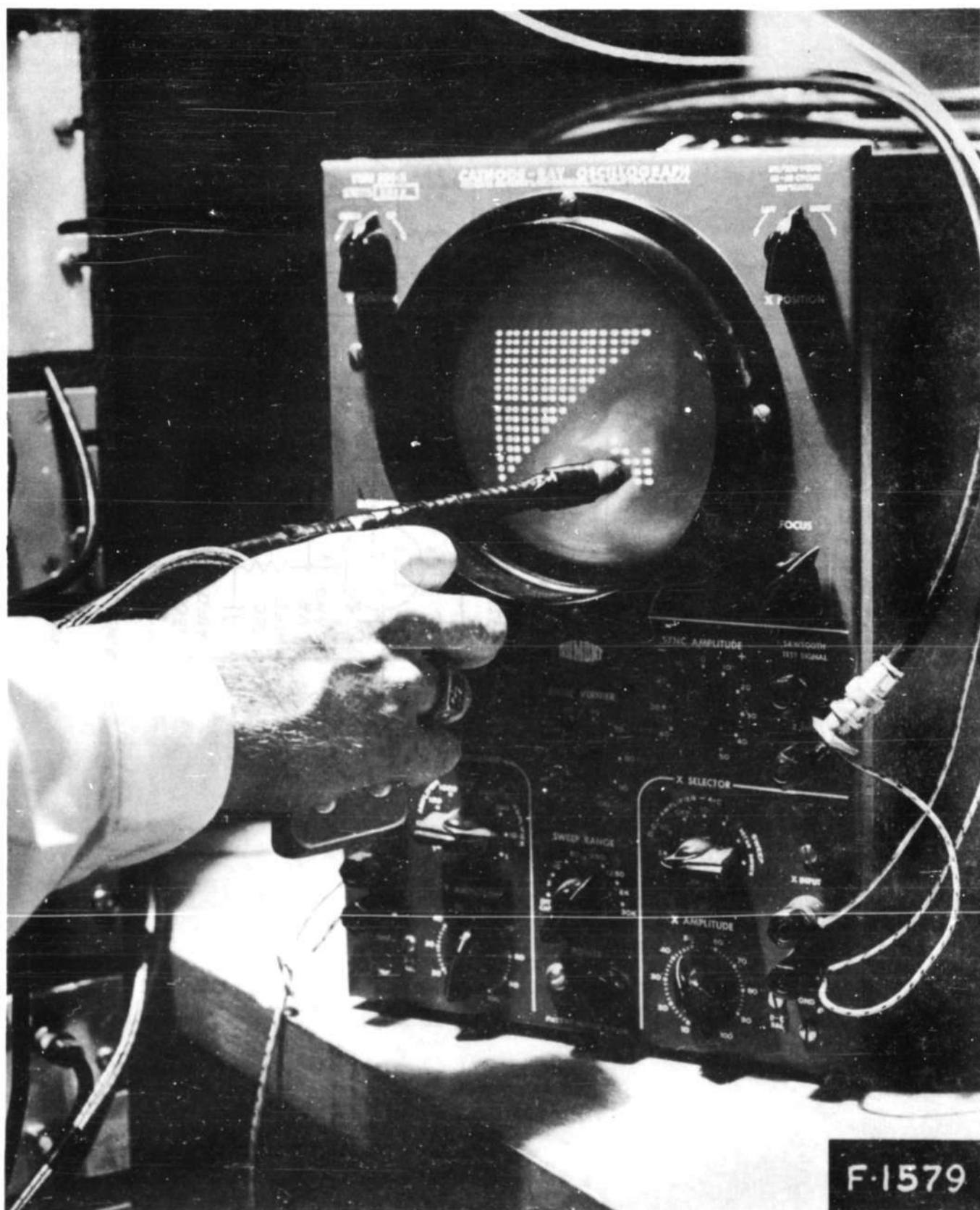
The basic test system of the magnetic memory showing connections of drivers and address selectors may be seen in Fig. 16. Included is a gate and delay unit between G&D #1 and GT #1. This unit allows adjustment of the interval between the end of the read gate and the beginning of the write 1 gate. The master clock is a P5 synchroscope. Its pulse output must be standardized before it can be used to trigger the coder. This arrangement allows the array to be scanned at a 4-kilocycle PRF and avoids synchronization problems. When it was desired to run the array at a higher speed, a multivibrator pulse generator was used to trigger the coder.

The array was able to store random patterns of information (as presented on the display scope) that were stationary in time as scanning took place. The next section contains some special circuits that were added to the system in order to facilitate pattern writing and to allow more rigorous testing.

B. SPECIAL CIRCUITS

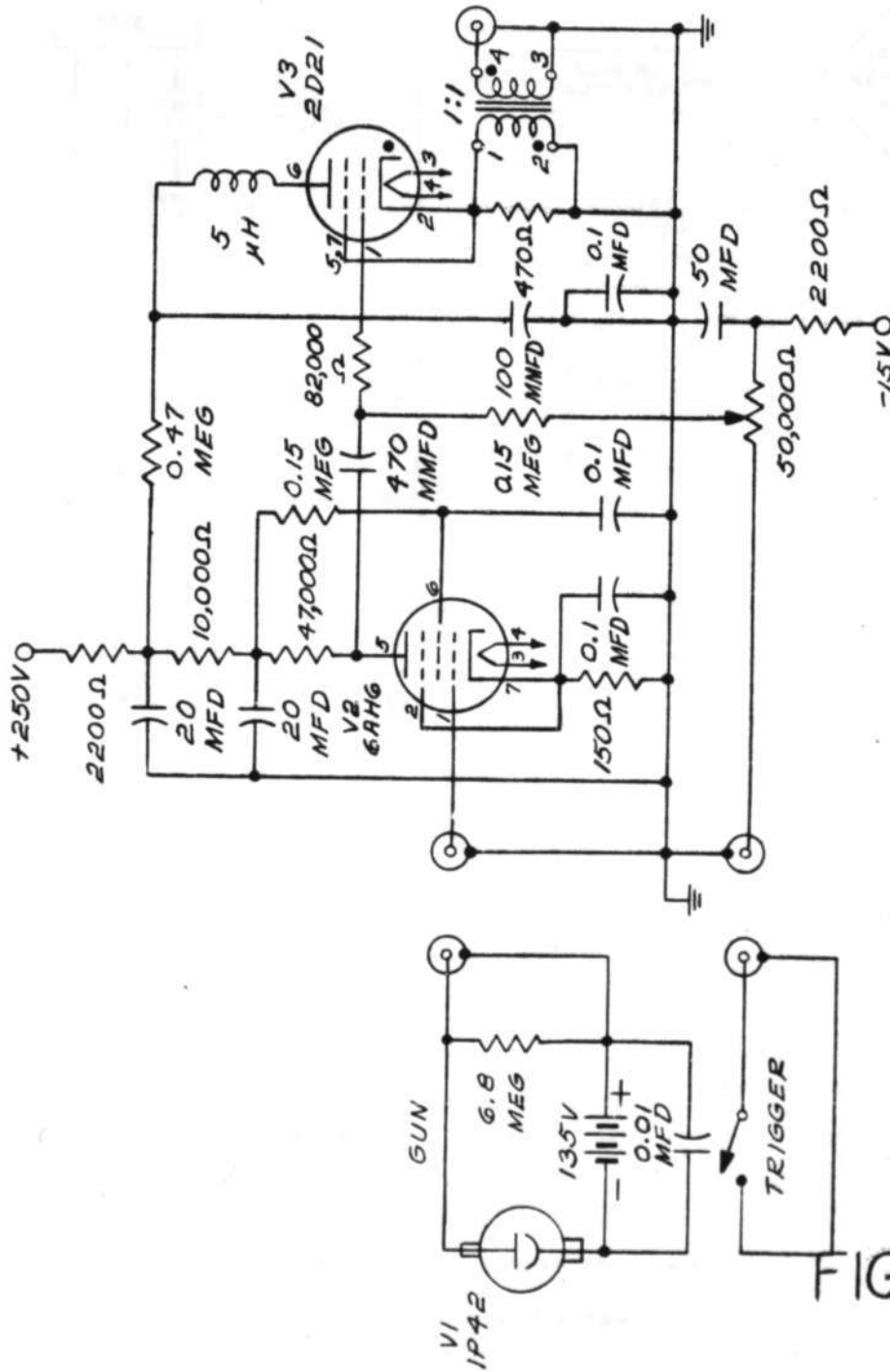
1. Light Gun

The light gun is a device for "shooting out" spots on the display scope. It simplifies the "writing" of arbitrary patterns by inserting "zeros" into a full array of "ones". Fig. 17 shows the light gun in operation.



A-52344

FIG. 17
WRITING PATTERNS WITH THE LIGHT GUN



CIRCUIT SCHEMATIC,
LIGHT GUN PULSE GENERATOR

A-51163

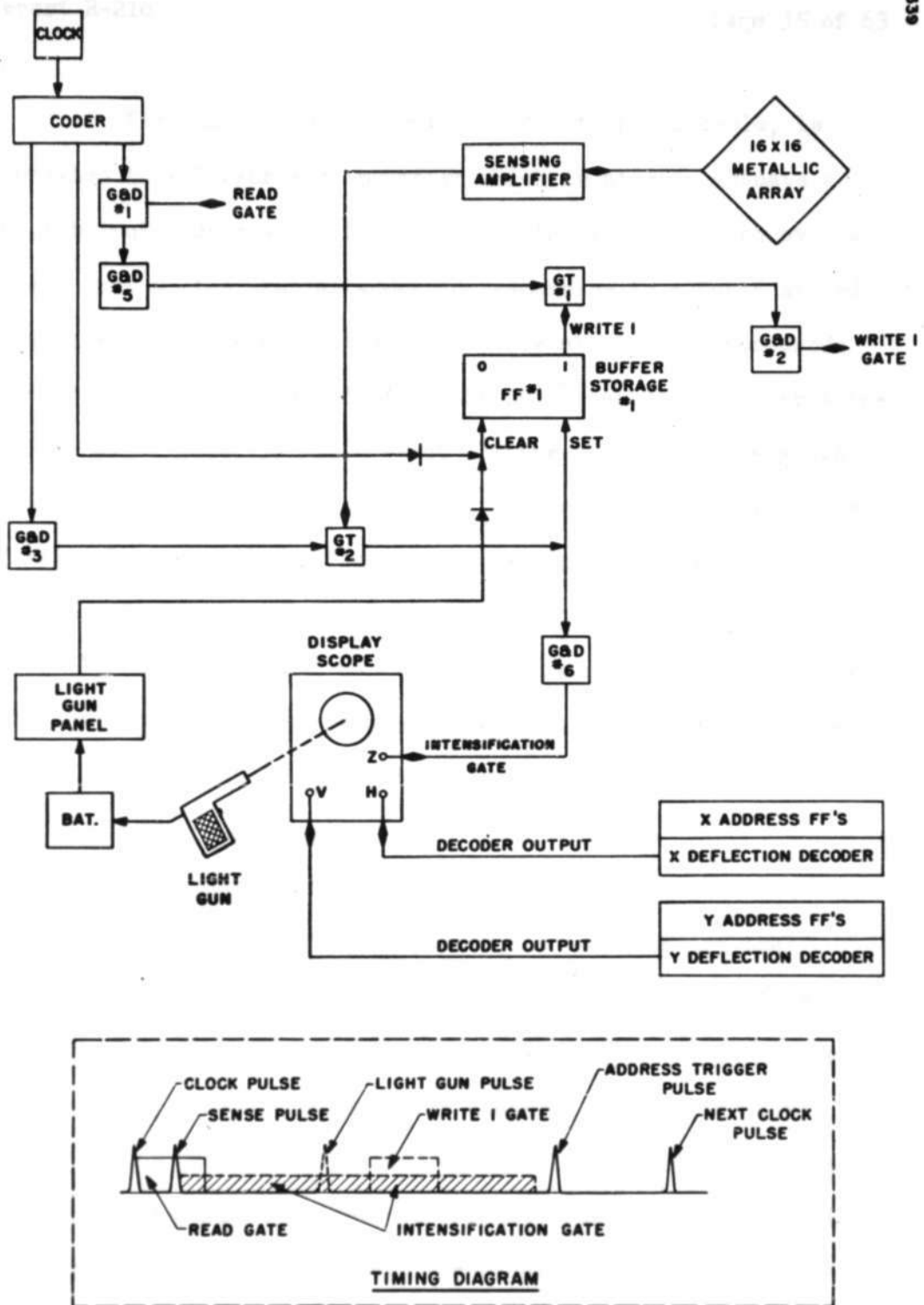


FIG. 19
BLOCK DIAGRAM
LIGHT GUN CONNECTIONS

The gun, a slender photocell built into a cable, is connected to a linear a-c amplifier which is able to actuate a gas tube pulse generator (Fig. 18). If the gun is placed over a bright spot on the display scope corresponding to a "one" stored in a core, it is able to give out a pulse about 15 microseconds after that spot is intensified. This pulse may clear buffer storage (FF #1, Figure 19) and prevent writing a "one" in the given core if the delay between the end of the read gate and beginning of write 1 gate (G&D #5, Fig. 19) is made greater than 15 microseconds. Once a "zero" is written in the core ("one" was not rewritten), the "zero" remains. That spot is no longer intensified.

Fig. 19 shows the block diagram of the light gun, the display scope, and associated equipment.

2. Moving Patterns

It is more difficult for a memory to hold a moving pattern than a fixed one. For the former, it is necessary that each core be able to remember both "zeros" and "ones". Addresses are scanned in the same manner, and the whole pattern is shifted one dot to the left for each raster scanned. This is done by writing into a core what was read out of the previously operated-upon core. Two buffer flip-flops are now necessary; one to hold the latest information read out, the other to hold the next-to-latest information (see Fig. 20).

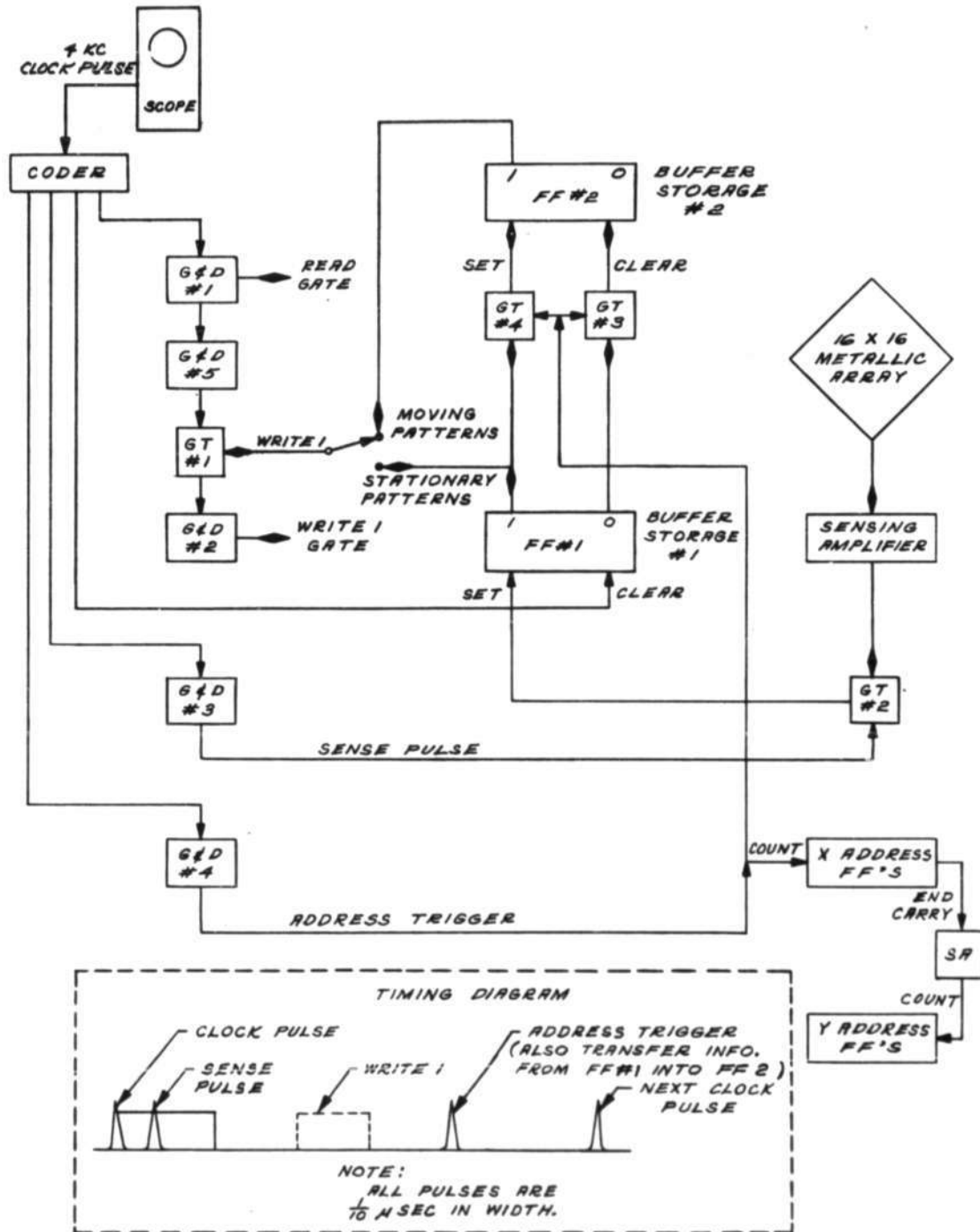


FIG. 20
BLOCK DIAGRAM,
MOVING PATTERNS SYSTEM

Flip-flop #1 is connected as before, and may be switched in to provide stationary patterns by connecting its "1" output to GT #1. FF #1 is cleared upon incidence of the clock pulse, remains cleared until the time of the sensing pulse, then is either in the "0" or "1" position (depending on whether the core contained a "0" or a "1") until cleared by the next clock pulse. During that time, the address FF's were set up on the next address. FF #2 is coupled to FF #1 through GT's #3 and #4. These gate tubes are pulsed at the time when the address FF's are triggered to the next address. This is done for convenience, to save a delay unit, and sets FF #2 to the number contained in FF #1. This number remains in FF #2 all the while the X and Y flip-flops are on the next address. Hence, if FF #2 is allowed to control GT #1, it becomes possible to write into a core the state of information of the core before. The display scope is connected as before, so that it always shows what was just read out. In the moving pattern mode, the pattern on the display scope "moves" because it is shifted one spot to the left each raster.

3. Skip Circuit

In a 16×16 array where the cores experience TV scanning, the maximum number of times that a given core may be disturbed before its information is refreshed is $2(n-1) = 30$, where n is the number of cores along a linear dimension. In order to allow an indefinite number of disturbances before a core is read, provision was made to skip this core during the normal scanning cycle. The array

could then be left running for hours, and the skipped core would be disturbed millions of times before its information was rewritten.

The circuit used is shown in Fig. 21. Clip leads connected to the suppressor grids of GT #5 and GT #6 are attached to outputs of the X and Y crystal matrices corresponding to the X and Y lines of the core to be skipped. A pulse delayed 1 microsecond relative to the regular address trigger will get through the gate tubes and trigger the address flip-flops to the next address only when the selected matrix outputs are those to which the clip leads are tied. The timing diagram (Fig. 21) shows how the double trigger is able to cause a skip and have the address flip-flops set up before the next read gate is begun.

4. Flip-Flop and Delay-Line Generators

Gate and delay units were used as the read and write-1 gate generators in the block diagrams shown thus far. They provided 40-volt gate inputs to the switch panels, allowed wide range adjustment of gate widths, and made operation simple. Their chief shortcoming, however, was their inability to maintain constancy of gate width during line transients. This was not serious until the array was run at high speed with a 3-to-1 selection ratio. Here, current gate widths were reduced to a minimum. Any jitter in the gate and delay units caused error. In order to allow high speed operation, it became necessary to use more reliable gate generators.

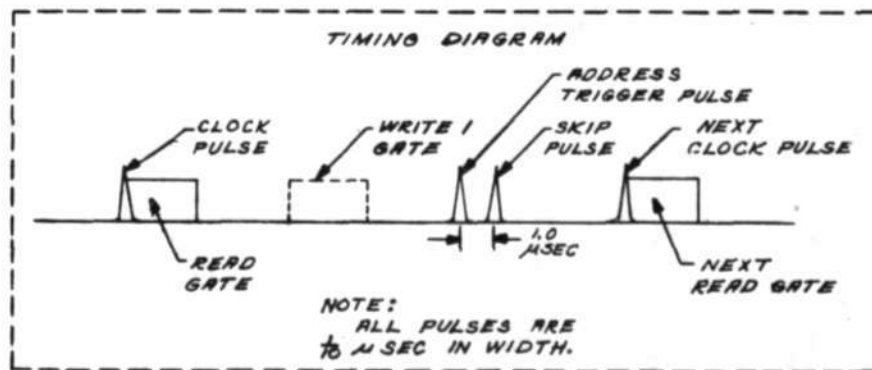
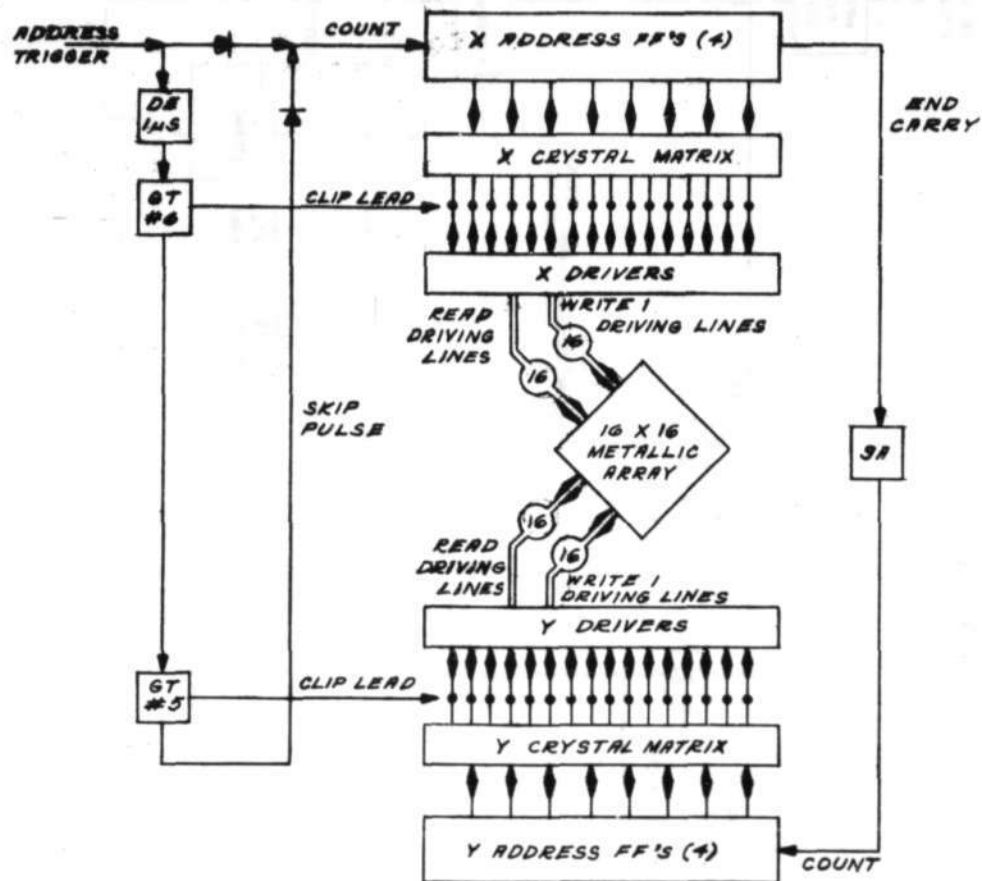


FIG 21
BLOCK DIAGRAM,
SKIP CIRCUIT CONNECTIONS

B-52209

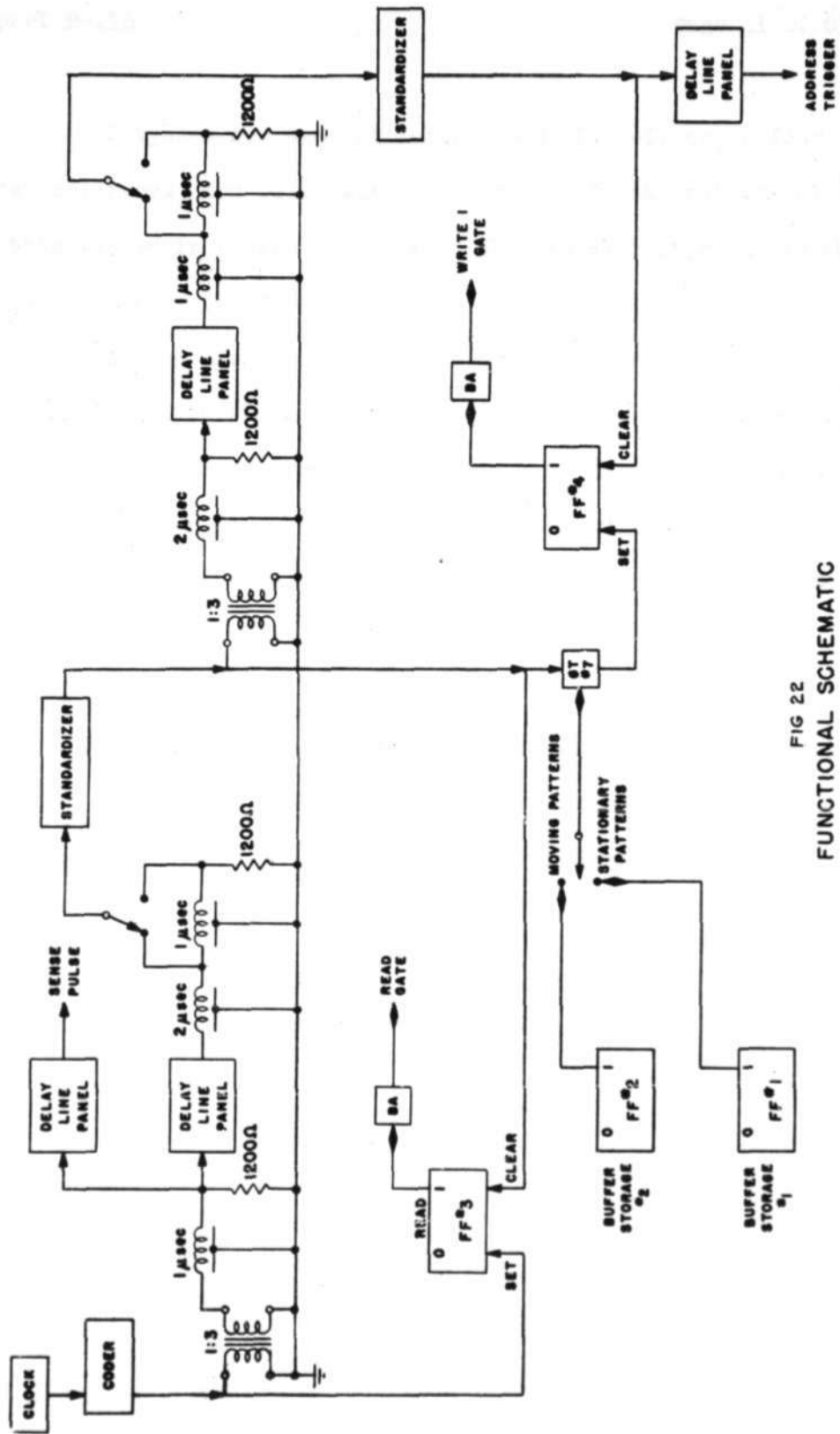


FIG 22
FUNCTIONAL SCHEMATIC
FLIP-FLOP AND DELAY LINE
TIME BASE AND GATE GENERATOR

A system was made of delay lines, flip-flops, buffer gate amplifiers, and pulse standardizers. A functional schematic of this system is shown in Fig. 22. When in use, it replaces the fundamental circuit of Fig. 15.

A time base is established by the delay lines and delay line panels. Each clock pulse yields a read gate, a sensing pulse, and an address trigger which is delayed long enough to allow for a write 1 if called for. GT #7 controls the initiation of the write 1 gate. The gate tube in turn is controlled by bugger storage FF #1 or FF #2 giving stationary or moving patterns.

3. Complete Block Diagram

Fig. 23 is a complete functional schematic of the metallic array as of July 1952. This diagram includes all of the information given in previously cited block diagrams.

0-87394

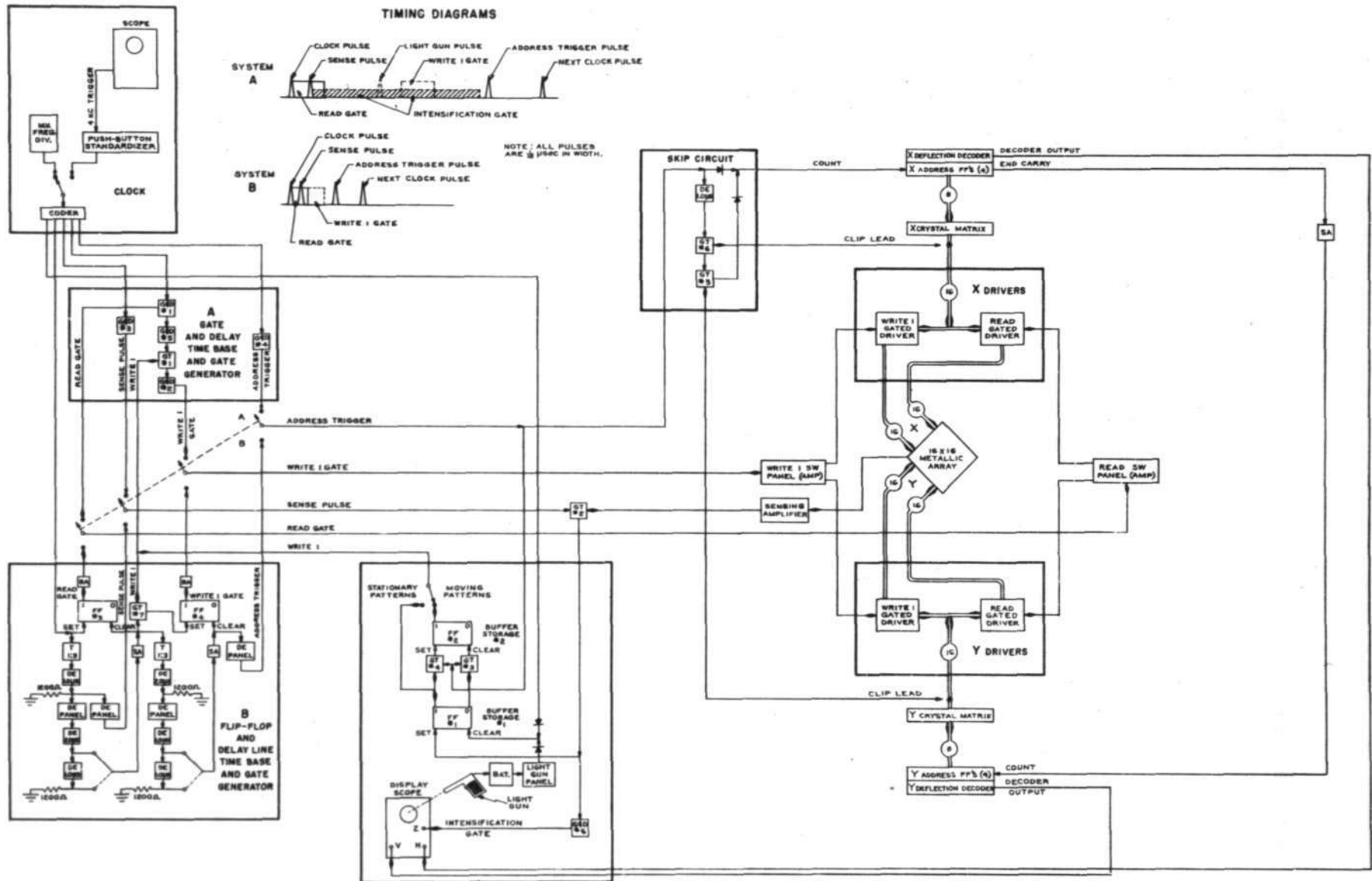


FIG 25
FUNCTIONAL SCHEMATIC, 16 X 16 METALLIC ARRAY

VI - OPERATING CHARACTERISTICS

The earliest testing was done by connecting one X and one Y driver to the array by clip leads. This allowed manual address selection, and was done before the flip-flop address selectors were set up.

When the X-address-selecting flip-flops and crystal matrix were de-bugged, a "16 x 1" array was run. Later, the X-address-selectors were able to be used, and full 16 x 16 operation took place.

The magnitude of driving currents used for the 1 x 1 operation was too large for coincident-current selection. 16 x 1 operation was possible only when these were reduced to the extent that non-selecting current disturbances were tolerable. When 16 x 16 operation was desired, it was necessary to increase the negative bias and the swing of the sensing panel output. Deviations in the outputs of the 256 cores were greater than was the case with only 16 cores being sensed, and this required a more careful adjustment of the sensing panel.

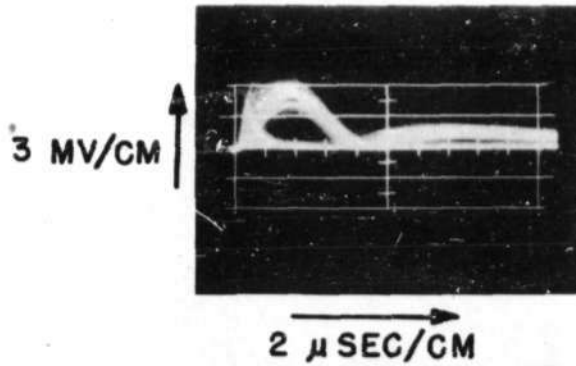
The preceding work was done with the block diagram of Fig. 16, using a 2-to-1 selection ratio. From there on, more logical equipment was added until the system represented in Fig. 23 was built up and operated. The next section contains some quantitative and qualitative operating characteristics that were derived during the first six months' run.

A. DRIVING-CURRENT WAVEFORMS

It is possible to look at waveforms of driving currents in the X and Y memory lines by observing the voltages developed across the 33Ω damping resistors in series with each line. The current drivers are nearly ideal current sources (Figs. 9 and 10), so that the back voltages of the memory lines (approximately $\frac{1}{2}$ volt peak on X and Y, 10 volts peak on Z) have negligible effects upon the current waveforms.

B. OUTPUT WAVEFORMS OF SENSING AMPLIFIER

Figure 24-1 is a composite of 256 traces showing the output of the sensing panel when the array is holding the pattern of Fig. 24-2 and is being cycled at a PRF of 4 kilocycles. The selection ratio is 2-to-1, with $I_m = 280$ milliamperes. Fig. 24-3 is the voltage at the input in the phase inverter of the sensing amplifier. This shows the positive and negative going signals induced in the sensing winding after going through linear amplification. Notice the variance in the amplitude of the ONES and ZEROS. Fig. 24-1 should be compared with Fig. 24-3, keeping in mind the sensing amplifier schematic, Fig. 11. Fig. 25 shows the output of a single type-B core containing a "zero" and a "one" (composite). The notch on the ONE output shows the incidence in time of the sensing pulse applied to the gate tube (GT #2) of Fig. 16 or Fig. 23. It is caused by suppressor current loading down the output of the sensing panel.



OUTPUT OF SENSING AMPLIFIER.
256 TRACES SHOW
ONES AND ZEROS

FIG. 24-1

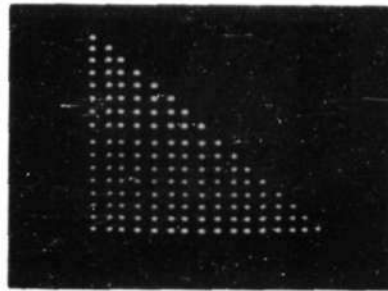
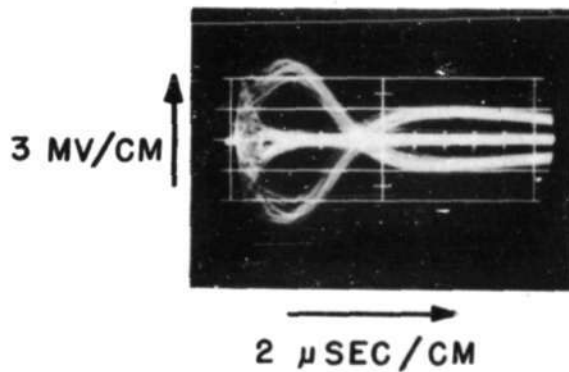


FIG. 24-2



INPUT TO PHASE INVERTER
OF SENSING AMPLIFIER.
THE OVERSHOOT IS DUE
TO A-C COUPLING IN
THAT AMPLIFIER.

FIG. 24-3

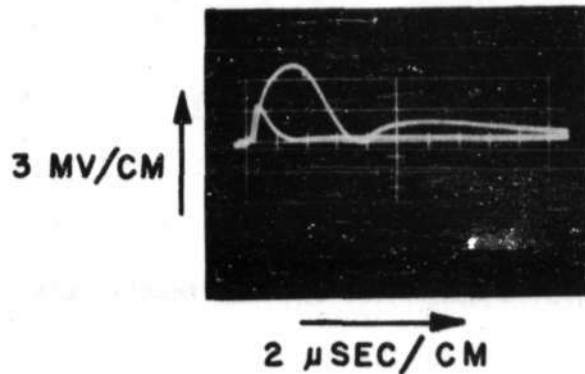
ARRAY WAS RUN AT A PRF OF 4 KC
WITH 2:1 SELECTION.

$I_x = I_y = 140$ MA

OPTIMUM SENSING TIME = 4.33 μSEC

FIG. 24

SENSING AMPLIFIER WAVEFORMS
WHEN ARRAY STORES A DIAGONAL PATTERN



255 CORES HOLDING "ones"
ADDRESS FLIP-FLOPS STOPPED AT
THE ADDRESS X=8 } CORE # 290
 Y=10 } TYPE B
SHOWN IS A ONE AND A ZERO
OF THIS CORE.

ARRAY WAS RUN AT A PRF OF 4 KC
WITH 2:1 SELECTION.
 $I_x = I_y = 140$ MA
OPTIMUM SENSING TIME = 4.33 μSEC

FIG. 25

ONE AND ZERO OUTPUTS
OF SENSING AMPLIFIER DURING READ-OUT
OF A TYPE B CORE

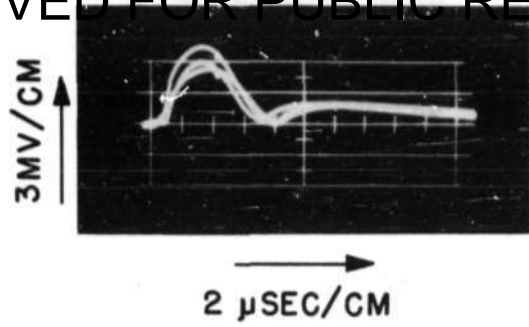
1. Variations in Sensed Outputs

The ONE outputs of the cores in the array were not identical in magnitude; neither were the ZERO outputs. The most significant reasons for these differences are:

a. Variations in magnetic properties of the individual cores are inherent in manufacture and are limited only by selection based on single core pulse test characteristics. Fig. 26-1 shows the ONE sensed output, while Fig. 26-2 shows the ZERO sensed output of typical types B, B-, and BC, since the rest of the array holds "ones".

b. Changes in I_m cause variation, because the output voltage varies almost linearly with I_m in the normal ranges of operation. This is not troublesome if driving current magnitudes are constant. These variations, which are applied to all the sensed cores, affect current margins. A sequence of photographs showing these variations for a 2-to-1 current-selection ratio for various values of I_m is shown in Fig. 27-1. Fig. 27-2 shows a similar set for 3-to-1 current selection.

c. Variations are sometimes caused by geometric irregularities of the array. The array was designed to minimize the mutual inductance between the sensing winding and all of the driving windings. If those windings were perfectly symmetric, the mutual inductance would be zero. Actually, this was not possible, so that voltages induced by the cores are superposed with those due to mutual coupling



ONES

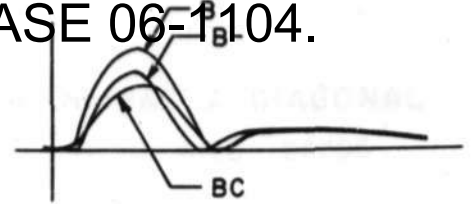
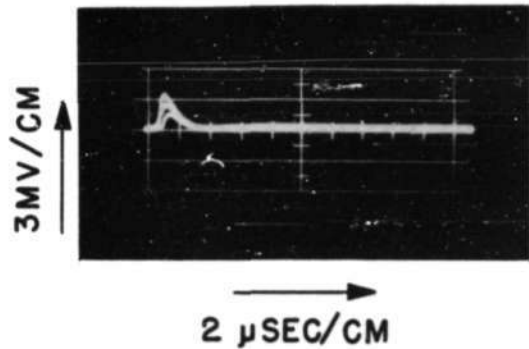


FIG. 26-1



ZEROS

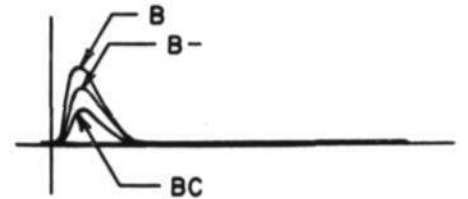


FIG. 26-2

ARRAY WAS RUN AT PRF OF 4KC WITH 2:1 SELECTION.
 $I_x = I_y = 140 \text{ MA.}$
 OPTIMUM SENSING TIME = $4.33 \mu\text{SEC.}$
 TIME BASE = $2 \mu\text{SEC/CM.}$
 ARRAY HOLDING ALL "ones" EXCEPT CORE SPECIFIED.

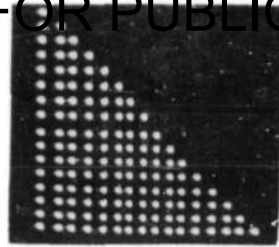
TYPE B: CORE #290, X=8; Y=10

TYPE B-: CORE #259, X=8; Y=11

TYPE BC: CORE #315, X=8; Y=9

FIG. 26

DIFFERENCES IN SENSED ONES AND ZEROS
 OF CORE TYPES B, B-, BC



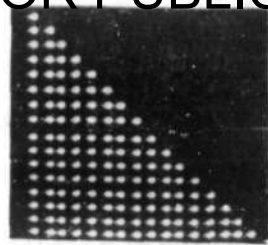
MEMORY PATTERN WAS A DIAGONAL PATTERN OF "ones" AND "zeros"

DRIVER RISE TIME $\frac{1}{2} \mu\text{sec}$

	X AND Y CURRENT	OPTIMUM SENSING TIME
	150 MA	4.33 μsec
	140 MA	4.66 μsec
	130 MA	5.00 μsec
	125 MA	5.33 μsec
	115 MA	5.50 μsec

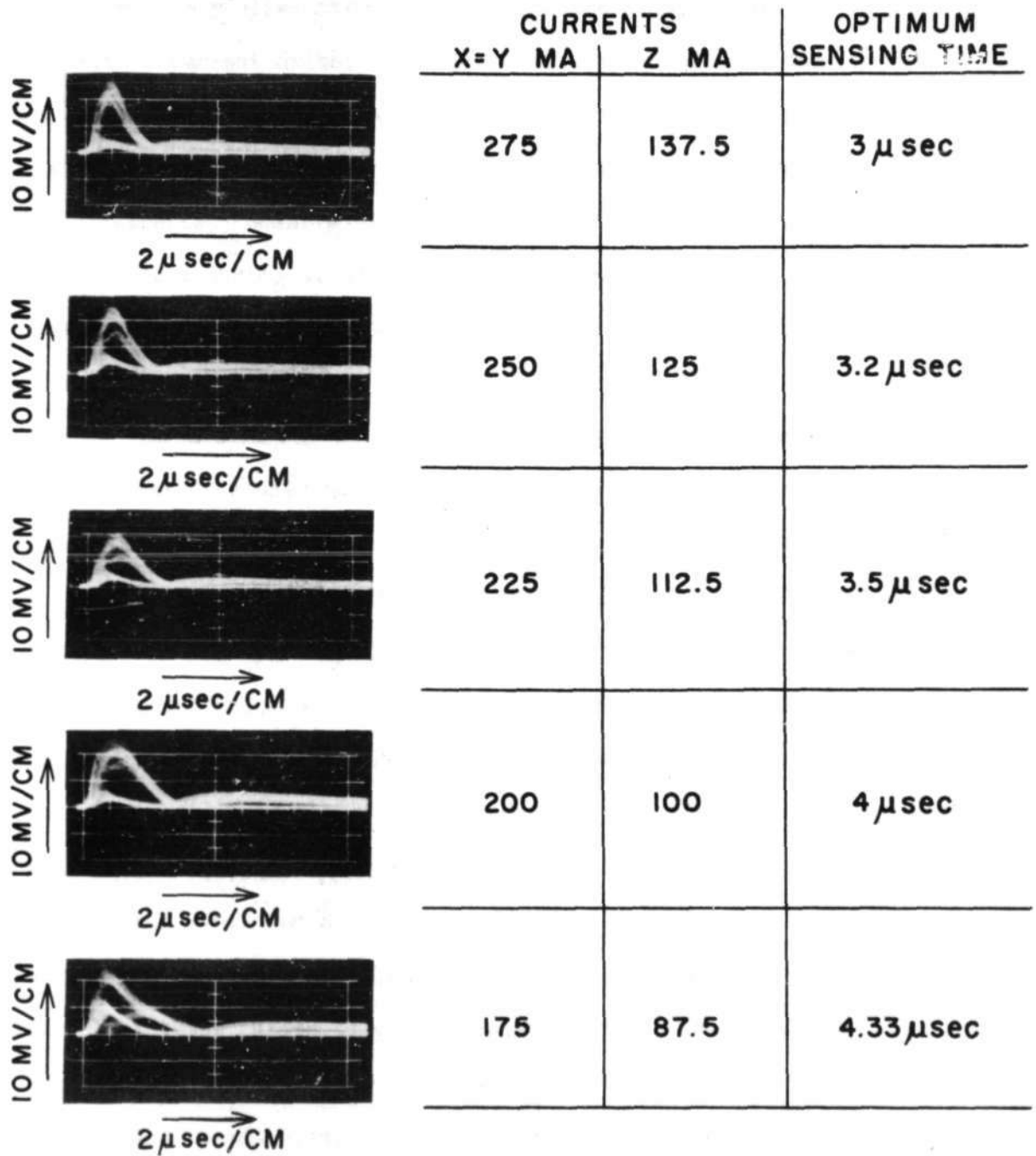
OPERATING 2:1 CURRENT SELECTION

FIG. 27-1 SENSING AMPLIFIER OUTPUT WAVEFORMS FOR VARIOUS VALUES OF I_m



MEMORY PATTERN WAS A DIAGONAL PATTERN OF "ones" AND "zeros"

DRIVER RISE TIME $\frac{1}{2} \mu\text{sec}$



OPERATING 3:1 CURRENT SELECTION

FIG.27-2 SENSING AMPLIFIER OUTPUT WAVEFORMS FOR VARIOUS VALUES OF I_m

across the sensing winding. Another factor is capacitive coupling between the driving lines and the sensing winding, which cannot be completely eliminated no matter how the windings are placed. With a current driver rise time of 0.2 microseconds, the voltage induced in the sensing winding by the Z-read winding is about half the size and shape of a typical ZERO when the Z current is 150 milliamperes. Under similar conditions, the Z-write 1 current would induce almost twice as much noise. Noise due to X and Y read and write 1 currents was found to be about 10% of the size of that due to the Z-write 1 current.

d. Variations may be due to the particular "zero" and "one" constellations stored in the memory. Not always does a given core (having fixed magnetic properties and geometrical position) produce the same size ZERO and ONE. The number and sequence of disturbances per raster depend upon the information pattern. The shape of a core's readout signals depends upon its history of disturbances from the time when the information was freshly written. More significant noise contributors are the non-selected readout-pulses of cores which may contain "zeros" (NS_0) or "ones" (NS_1). These cores have their X or Y line common with the selected core and are disturbed during reading or writing 1. The sensing winding is wound to cause all of these pulses to cancel, except for 2. This would be so if all cores yielded the same size non-selected pulses. They do not, however, and in addition, a given core will produce a larger non-selected pulse if it contains a "one" than if it contains a "zero".

The non-selected pulses have about the same shape and size as ZEROS. This is fortunate, because they decay away to 10% of peak before the sensing time occurs. Stored patterns were designed to emphasize the effects of differences in non-selected outputs upon sensed waveforms, and it was found that these differences seriously impair ONE-ZERO discrimination in a 256-bit memory with 3-to-1 selection (Z used for driving), and make operation almost marginal with 2-to-1 selection. The effect clearly places a limitation on the number of cores that may be sensed with the type of sensing winding used. Even when the induced noise is over before the sensing time, the transient has an effect upon an a-c-coupled sensing amplifier which may be troublesome in large arrays.

Fig. 29 shows ZEROS and ONES of a type-B core, the selected core where the three display scope patterns of Fig. 28 were stored to give either no noise or the maximum possible values of noise of both senses. The difference between the largest ONE and the ONE without noise (shown in Fig. 29-1) is approximately the same as that between the ONE without noise and the smallest ONE. This difference is equal to 14 times the difference between the non-selected output of a core containing a "one" (NS_1) and a "zero" (NS_0). Fig. 29-2 exhibits the same differences with the selected core containing a "zero" instead of a "one" as in Fig. 29-1. Fig. 30-1 shows the ONE output of the sensing amplifier while the patterns of Fig. 28 were stored with a 2-microsecond rise time instead of a $\frac{1}{2}$ -microsecond rise time.

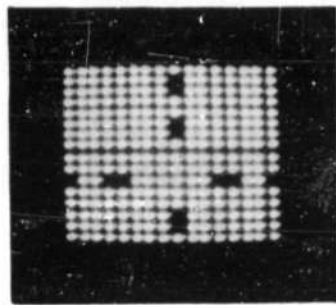


FIG. 28-1

PATTERN TYPE 1

ASSUMING LIKE CORES, THIS PATTERN DOES NOT INTRODUCE NON-SELECTED NOISE IN SENSING WINDING WHEN SELECTED "X" AND "Y" LINES ARE PULSED.

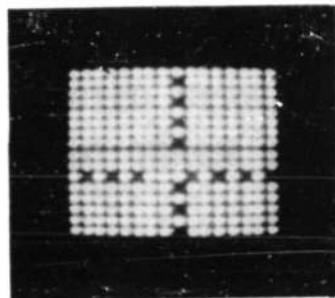


FIG. 28-2

PATTERN TYPE 2

INTRODUCES NOISE TO MAKE SELECTED CORE "one" OUTPUT LARGER.

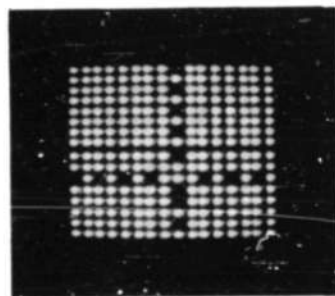


FIG. 28-3

PATTERN TYPE 3

INTRODUCES NOISE TO MAKE SELECTED CORE "one" OUTPUT SMALLER.

SELECTED CORE, #290, TYPE B, IS AT THE INTERSECTION OF LINES $X=8$, $Y=10$.

FIG. 28

DISPLAY OF STORED PATTERNS DESIGNED TO EMPHASIZE THE EFFECTS OF NON-SELECTED READ-OUT NOISE

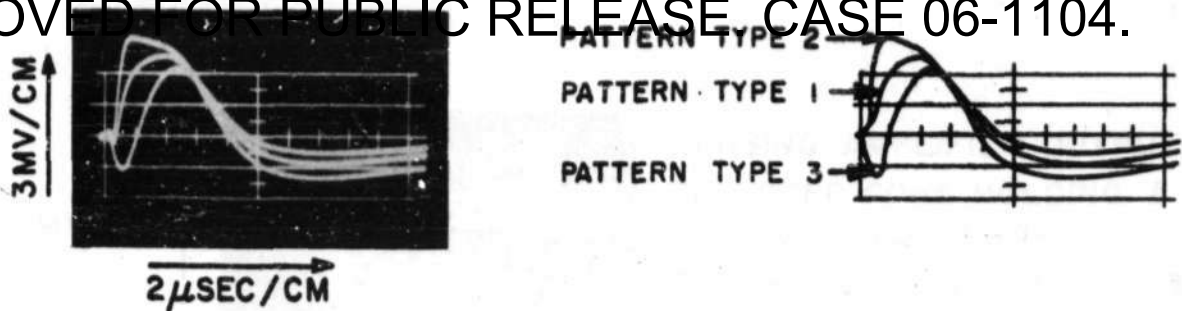


FIG. 29-1

SELECTED CORE HOLDING A "one"
FOR PATTERN TYPES 1, 2 AND 3
OF FIGURE 33.

SELECTED CORE TYPE B, #290, X=8, Y=10
OUTPUT TAKEN AT PHASE INVERTER INPUT OF SENSING AMPLIFIER.

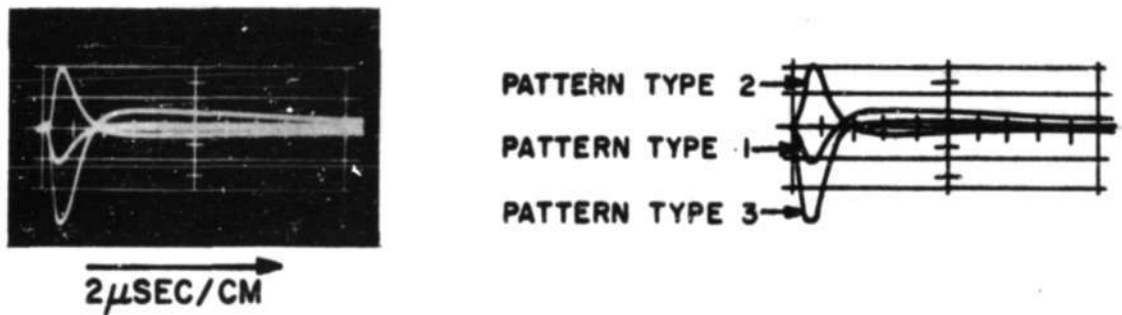


FIG. 29-2

SELECTED CORE HOLDING A "zero"
FOR PATTERN TYPES 1, 2 AND 3
OF FIGURE 33.

SELECTED CORE TYPE B, #290, X=8, Y=10
OUTPUT TAKEN AT PHASE INVERTER INPUT OF SENSING AMPLIFIER.

ARRAY WAS RUN AT A PRF OF 4KC WITH 2:1 SELECTION.

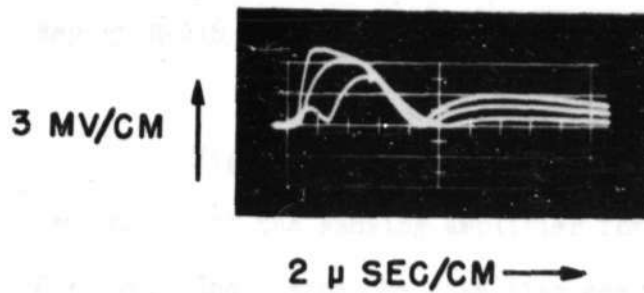
$I_x = I_y = 130 \text{ MA}$

RISE TIME OF DRIVER $\frac{1}{2} \mu\text{SEC.}$

OPTIMUM SENSING TIME $4.33 \mu\text{SEC.}$

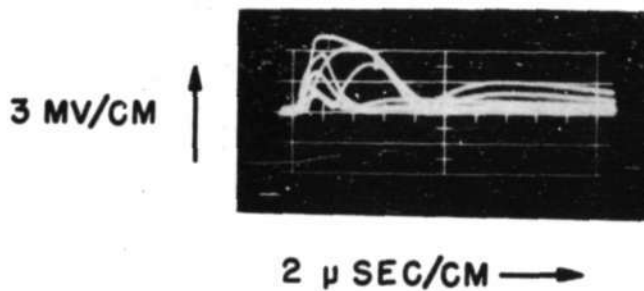
FIG. 29

ONE AND ZERO INPUTS TO SENSING AMPLIFIER PHASE INVERTER
WITH ARRAY STORING PATTERNS OF FIGURE 33



SENSING AMPLIFIER OUTPUTS,
SELECTED CORE HOLDING A
"one" FOR PATTERNS
TYPES 1, 2, AND 3 OF FIG. 33.

FIG. 30-1



SENSING AMPLIFIER OUTPUTS,
SELECTED CORE HOLDING "one"
AND "zero" FOR PATTERNS
TYPES 1, 2, AND 3 OF FIG. 33.

FIG. 30-2

2 TO 1 SELECTION.

$I_x = I_y = 130$ MA.

OPTIMUM SENSING TIME 5 μ SEC.

SELECTED CORE TYPE B, NUMBER 290, X=8, Y=10.

RISE TIME OF DRIVERS INCREASED TO 2 μ SEC.

FIG. 30

SENSING AMPLIFIER OUTPUTS
WHEN PATTERNS OF FIG. 33 ARE STORED

Fig. 30-2 is a composite of the ONES and ZEROS at the output of the sensing amplifier for the three patterns of Fig. 29. Increasing the rise time seems to have little effect upon the noise produced by the non-selected cores.

2. Standard Output

Since the shape of the output pulse of the sensing amplifier affects operating margins, it was necessary to establish standards so that the experimental data would be reproducible. It was decided that the gain of the sensing amplifier be set to give an output of 30 volts above bias for the smallest ONE (found by reading all "ones" into array) at the time of sensing. The output bias was set at -30 volts, and the 1/10-microsecond pulse applied to the control grid of GT2 of Fig. 23 was 30 volts high.

3. Optimum Sensing Time

A time always occurs when the ratio of the amplitude of the smallest ONE output of the sensing amplifier to the largest ZERO is maximum. This time is different for each of the 2^{256} possible patterns of stored information. Fortunately, it turns out that there exists a region of time about this point over which the ZERO-to-ONE ratio is almost constant. This region is usually one microsecond wide for a 20% deviation from maximum. For a given selection ratio (2-to-1 or 3-to-1), and for given current levels, it was possible to find by inspection of sensing panel waveforms some optimum sensing point that would be within this region for all the patterns stored. A plot of this optimum point in time for 2-to-1 current selection ratio is shown in Fig. 31.

A - 52314

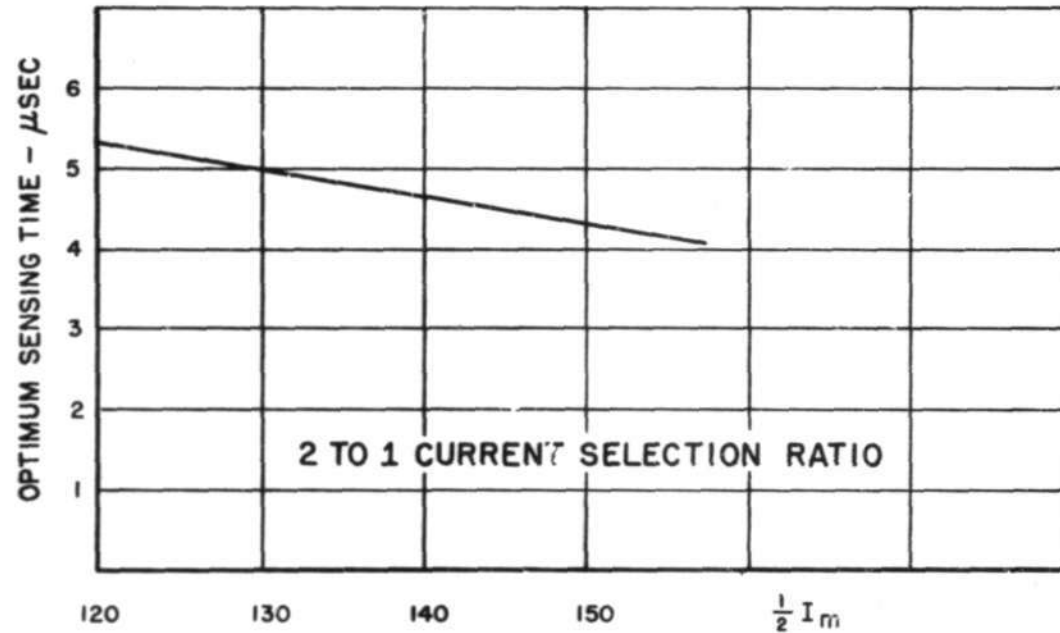


FIG 31
OPTIMUM SENSING TIME
(TIME WHEN INFORMATION IS AVAILABLE AFTER READING BEGINS)
vs $\frac{1}{2} I_m$

DATA TAKEN
ON AUGUST 12, 1952

C. SPEED OF OPERATION

The read-rewrite time, the smallest allowable time interval between the asking for a bit of information and the asking for a subsequent bit of information, is determined mainly by the time necessary to switch a core and, to a small extent, by the delays inherent in address flip-flop and crystal matrix set up time and by delays in the current drivers (including rise times). Readout time, or the time after the asking when the desired information is available, is the optimum sensing time, a function of the mode of operation, and the transient response of the sensing amplifier.

Switching time of a core may be measured by observing the sensed waveforms. The core may be considered switched when its output voltage is zero. In order to switch a core completely, the driving current gate must be equal to or greater in length than the time required for switching voltage to go to zero. If the current gate is shortened from this critical time, the sensed waveform changes; if lengthened, no change is experienced. The sensing panel, an a-c-coupled amplifier, does not permit a simple way of measuring switching time because of overshoot, but it does allow detection of change. The actual point of zero output of the sensing panel may not correspond to the end of switching. Switching times were measured by observing the durations of the read and write 1 current gates while monitoring the sensing amplifier waveforms.

When a core in the memory is to be set in either state, the information should always be read in by full-length write-0 or write-1 gates. The memory may be greatly speeded up, however, by squeezing in the current gate durations during a read-rewrite cycle.

The reading, or writing-0 operation, needs only to be carried on until the time of incidence of the sensing pulse. If the core was in the "zero" state, the reading, whether done by a long or short current, will still indicate the "zero" state. If the core was in the "one" state, it will soon be reset to that state, and the time required for this is less than if long gates were used in the reading operation. The procedure for adjusting the memory for the highest speed at given values of driving currents is the following: Set the sense pulse at the optimum sensing time. Reduce the read current gate width until the sensing amplifier output waveforms begin to be distorted at the optimum sensing time by the noise induced in the sensing winding when the read currents are shut off. The shortest allowable read current gate is usually 1 microsecond longer than the optimum sensing time. Now shorten the write-1 current gate until the amplitudes of the ONES at the sampling point are reduced to 90% of their peak values. Fig. 32 shows the minimum allowable read and write-1 times as functions of $\frac{1}{2} I_m$ for a 2-to-1 current-selection ratio. That the array was able to cycle random moving patterns is what is implied by "allowable". These times or current gate widths were measured as the intervals between those points at which the driving currents have risen and fallen to half their steady state values.

In order to estimate the minimum time required for a read-rewrite cycle with a given selection ratio, rise time of drivers, and I_m , the following calculations should be made:

$$\begin{aligned} \text{min. read-rewrite time} = & \text{min. read time} + \text{min. write-1} \\ & \text{time} + \text{driver rise time} + \text{address flip-flop setup time.} \end{aligned}$$

There will be no delay between read and write 1. Since address setup requires $\frac{1}{2}$ microsecond, and if the driver rise and fall times are $\frac{1}{2}$ microsecond,

$$\begin{aligned} \text{min. read-rewrite time} = & \text{min. read time} + \text{min. write 1 time} \\ & + 1 \text{ microsecond.} \end{aligned}$$

Using shortened gates, the array was run at a PRF of 50 kilocycles with a 2-to-1 current-selection ratio.

D. MARGINS AND RELIABILITY

1. Current Margins

It is important to have the driving currents regulated in order to have reliable operation. If the driving currents are made larger or smaller than when originally adjusted, the optimum sensing time of the first situation may not be the same as that after subsequent changes. If the driving currents are made too large, the information in the non-selected cores may be destroyed by disturbances. Also, noise due to non-selected cores may be great enough to cause ZEROS to be mistaken for ONES. On the other hand, if the driving current magnitudes are made too small, the driving current gates may not be wide enough to allow complete switching of cores, and this may entail loss of information. Also, some of the ONES may be too small to actuate the sensing gate tube. (GT #2, Fig. 23).

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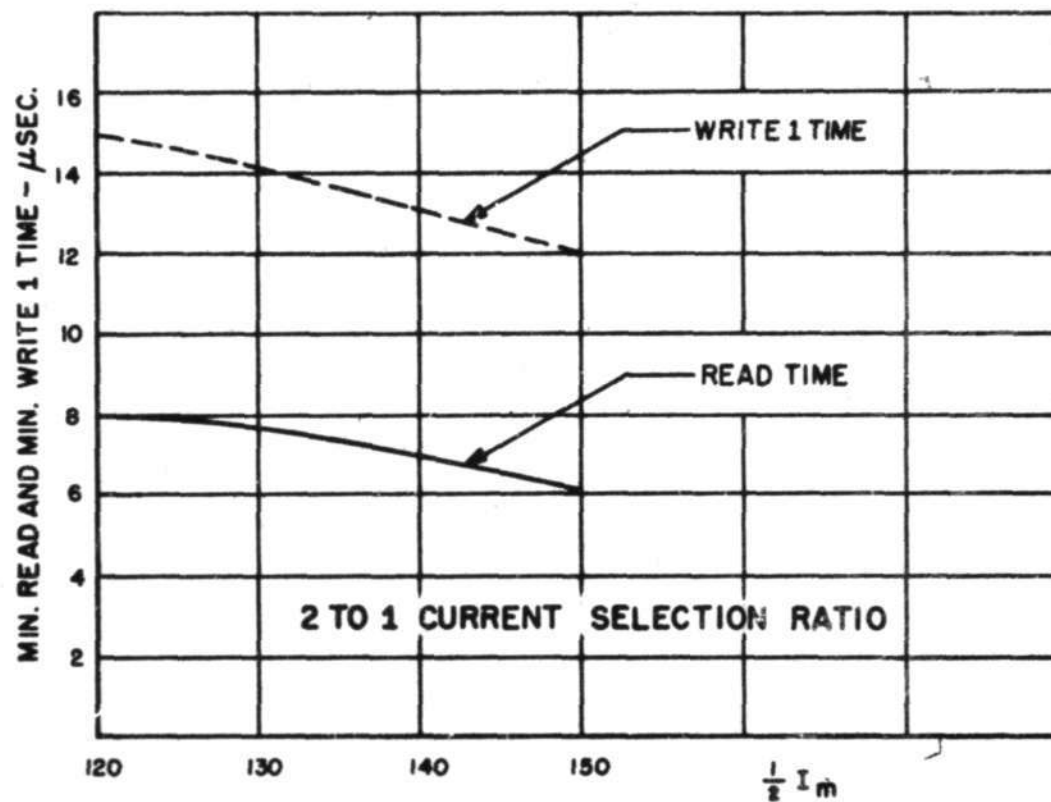


FIG 32

MINIMUM READ AND MINIMUM WRITE 1 TIMES

FOR READ RE-WRITE CYCLES vs $\frac{1}{2} I_m$

DATA TAKEN
ON AUGUST 12, 1952

Some quantitative data were recorded concerning the amount that these currents may deviate about a set value when the memory's adjustments were optimized for that value. This was done with a driver rise time of $\frac{1}{2}$ microsecond for various values of I_m with 25-microsecond read and write 1 current gates, 2-to-1 selection, and the sensing pulse occurring at the optimum sensing time for the given value of I_m . These data, taken by cycling random moving patterns at a PRF of 4 kilocycles, are shown in Fig. 33.

2. Reliability

The system has worked successfully for six months, logging several hundred hours of memory operation with a 2-to-1 current selection ratio. During this time, errors were found to have occurred only when the power supplies were hit by heavy transients or when the system was out of adjustment. In no case was it clear that the array of cores was responsible for an error. Moreover, no deterioration of the magnetic properties has, as yet, been detected.

Use of the delay-line flip-flop gate generators (system B of Fig. 24) improves stability when the memory is run at high speed with 3-to-1 selection. Sensitivity to line transients is greatly reduced, in that operation of the array with an 8-microsecond read-rewrite time is possible whereas with gate and delay gate generators (system A of Fig. 23), this would not be so. It was found, however, that certain types of patterns, those resembling checkerboards, could not be reliably stored with 3-to-1 current selection using the system.

of Fig. 23. The difficulty has been traced to non-selected noise produced by all cores linked by the "Z" axis winding except the selected core as discussed above. This noise may force a limitation upon the use of the "Z" winding during a reading operation.

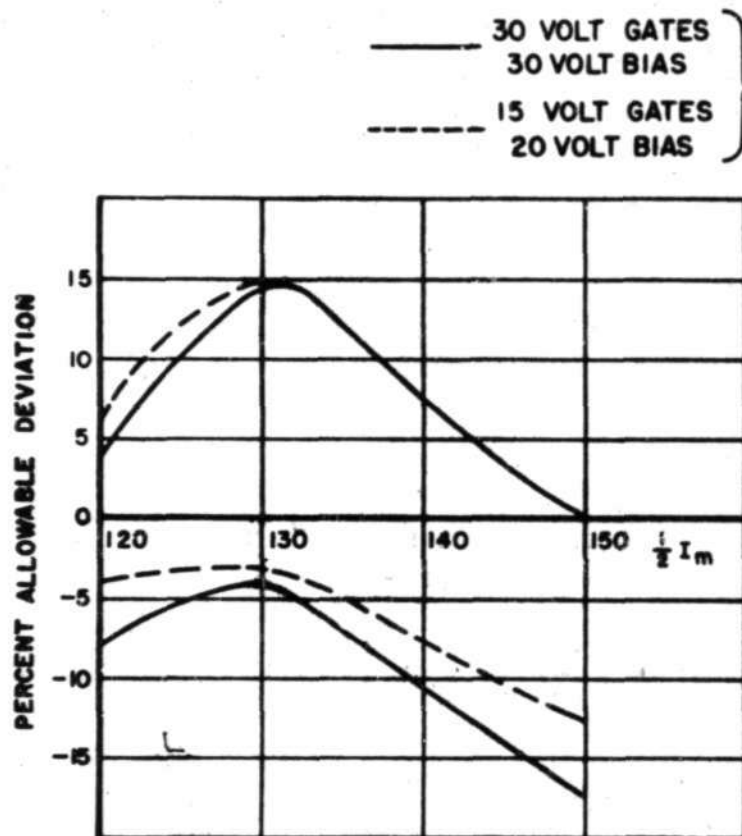
E. CONCLUSIONS

Evidence for the soundness of the concept and suggestions made in R-187 with respect to three-dimensional magnetic-core arrays has been gathered during months of testing on the 16 x 16 metallic memory. The results are encouraging for so early a stage of development of a new idea.

Two specific major problems which afflict the present array are the large variation in characteristics from core to core, and the uncanceled non-selecting output noise. Core variations can only be reduced by a high degree of quality control in manufacture and a rigorous preselection program. Uncanceled NS noise may be mitigated by improved core characteristics, by the use of multiple sensing windings and circuits, and by non-simultaneous application of the coordinate driving currents.

These problems will be studied on this array and others. Memory reliability is the first and main goal, and it is hoped that the information "put on the record" by this report will be of some small help.

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——— 30 VOLT GATES
 30 VOLT BIAS
 - - - 15 VOLT GATES
 20 VOLT BIAS

OUTPUTS OF SENSING AMPLIFIER

SENSING AMPLIFIER OUTPUT: 30 V GATE AT OPT. SENSING TIME, 30 V BIAS		
I_m ma	OPTIMUM SENSING TIME	SENSING AMPLIFIER GAIN
120	5 μ SEC	17,000
127	5 μ SEC	13,000
130	5 μ SEC	8,500
140	4 μ SEC	7,500
150	4 μ SEC	7,000

SENSING AMPLIFIER OUTPUT 20V GATE AT OPT. SENSING TIME, 15 V BIAS		
I_m ma	OPTIMUM SENSING TIME	SENSING AMPLIFIER GAIN
120	5 μ SEC	7,500
130	5 μ SEC	5,000
140	4 μ SEC	4,000
150	4 μ SEC	3,000

FIG 33
CURRENT MARGINS

DATA TAKEN
ON AUGUST 12, 1952

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