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June 27, 1955

ELECTRICAL ENGINEERING DEPARTMENT
MASTER'S THESIS PROPOSAL

TITLE: A TRANSISTOR SELECTION SYSTEM FOR A MAGNETIC-CORE MEMORY

STATEMENT OF THE PROBLEM

A multiposition transistor selection system is to be designed that will be operated by the 2n inputs from a transistor memory-address register and that will allow random selection of one of 2^n output lines. The selected output line is to present a low impedance to ground and be capable of conducting a stated range of current amplitudes that may or may not include both directions of current flow. The non-selected output lines must present a high impedance to ground.

HISTORY OF THE PROBLEM

In the development of electronic computers an important element was the system for selection of numbers or words in the memory. With the large storage capacity possible in the magnetic-core memory which was proposed in 1949 by J. W. Forrester,[1] an elaborate system became necessary to perform the random access selection. (Reference 2 and Fig. 1.1 give a fairly complete description of the operation of the memory.)

In general, selection information[3,4] for the magnetic-core memory is supplied by a n-binary-digit memory-address register which is followed by cathode followers on each of the 2n output lines (see Fig. 1.2). The cathode followers drive a diode matrix[5] which, for a given state of the memory address register, selects one of the 2^n output lines.

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Each output line drives an amplifier which in turn drives two AND gates. As is indicated in Figure 1.2, one of the AND gates in each output line is connected to a READ driver and the other AND gate in each output line is connected to a WRITE driver. When either of the drivers is turned on only one AND gate will be open and allow current to flow through a pulse transformer[6] which will couple the signal to the correct selection line.

With the development of the large (256 x 256 x 37) memory,[7] the reliability of the selection system depends mainly on the reliability of the vacuum tubes. Large heavy-duty tubes are required to handle the high currents (410 ma) needed for the ferrite core memory. Filament power must be supplied to all the tubes continuously and the resulting heat must be dissipated without damage to temperature sensitive components in the memory system. The necessary power cooling mechanism not only increases space requirements and total power input, but must be included in the reliability considerations of the complete selection system.

When the point-contact transistor appeared with its prospect of extreme reliability, long life, high efficiency and small size, computer engineers began to develope circuits that would replace the vacuum tube with its previously mentioned faults.[8,9] The point-contact transistor, however, has major defects such as low power dissipation, sensitivity to high temperature, sensitivity to humidity, and lack of uniformity. As a result, S. Oken of MIT in a Master's Thesis[9] reported that he was unable to drive the ferrite memory cores directly with

point-contact transistors or with early junction transistors. He did develop a core driver consisting of a point-contact flip-flop driving a grounded-base junction transistor (to increase the output impedance) that was capable of driving several metallic cores. Since the switching time of the metallic cores is 10 microseconds when used in coincident-current operation, reverse recovery problems were not as great as would be expected in a ferrite core memory with 1 microsecond operation. The supply voltage of the transistor driver must be high enough to keep the output current constant when the cores are switching and, as a result, the dissipation in the transistor will be high when the cores are not switching. Therefore, the number of cores to be driven is limited by the maximum dissipation of the transistor.

K. Olsen[10] has suggested using the transistor in the saturated state where dissipation will be low even if both READ and WRITE generators cause current to flow through the same transistor. The outputs of all the non-selected transistors will be subjected to the memory plane back voltage, but these transistors will be open circuited and there will be little or no dissipation.

R. Baker and R. McMahon of Lincoln Laboratory are also working on a scheme in which only the non-conducting transistor must absorb the back voltage. The main difference between the two schemes is that, in the first, the transistor is saturated and bilateral, and in the second, is non-saturated and unilateral. In the latter arrangement two transistors and a pulse transformer are required. Both systems require an external READ and WRITE current source.

The work of P. Gray[11] and others[12,13,14] on the transient response of junction transistors used as a current source provides a general indication of the circuit configuration having the shortest turn-on and turn-off time.

Some useful techniques have been obtained from the work of N. T. Jones[15] who tested the recovery time of point-contact transistors in terms of parameters which facilitate comparison of different units.

PROPOSED PROCEDURE

The transistor memory-address register that will be the input to the proposed selection system has already been designed by members of the computer development group at Lincoln Laboratory. The maximum output current and the output impedance are two parameters that will determine, in part, the circuitry that follows. Because the expected output current will be on the order of 1 ma, grounded emitter stages will be used to increase the current amplitude. There are three possible places for the amplification: before the matrix where there are 2n lines, after the matrix where there are 2^n lines and within the matrix where there are more than 2^{n+1} units.[16]

Since reverse recovery is a problem in diodes capable of carrying the 20 to 100 ma currents that are required to drive the selection transistor, it is unlikely that all of the amplification can take place before the diode matrix. If the selection transistor requires more than one driver after the diode matrix a transistor matrix will be considered as a possible element. Such a matrix will be desirable if it would

eliminate more diodes and transistors than it added, or if the response times are decreased.

The non-saturated mode of operation uses the transistor* in the grounded collector configuration. When one of the drivers is pulsed, current will flow into the emitter of the transistor that has the low base voltage. Since the emitter diode was floating prior to activation of the current source, it will take some time for the holes to diffuse to the collector. Therefore, the initial voltage drop and the instantaneous power dissipation will be high. When the current source is withdrawn, holes will recombine, but, with no field to aid the process, the base driver will still be the main element in the turn-off process unless the base is kept positive with respect to the collector even when this particular line is selected. Since this technique is being studied by another group at Lincoln Laboratory, this thesis will be directed towards the saturated mode of operation.

With the emitter grounded and a resistor connected from the collector to a negative supply, the collector current will be very small if the base current is zero. As the base current is increased the collector current will increase and the collector to emitter voltage will decrease. When the point is reached where increasing the base current will neither increase collector current nor reduce collector to emitter voltage, the transistor is said to be in saturation. The

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*The following discussion applies to PNP transistors.

ratio of collector current to base current at the transition point is the d-c saturation current gain, B_s. If a current source is connected to the collector instead of the resistor and battery, the circuit corresponds to the saturated configuration proposed by Olsen.[10] Let a step of base current be applied to the transistor and let a narrow pulse of current be forced out of the collector by the current generator. If the pulse of current occurs shortly after the base current, then the voltage from collector to emitter will not be the low d-c value. As the current pulse is delayed more, the collector voltage decreases exponentially to its low d-c value. The saturation current gain, B_s, is not constant but varies inversely with base current. The gain is not the same for both directions of collector current and is greater for current out of the collector. One of the first tasks will be to determine B_s as a function of the above parameters for various transistors.

If the transistor is used bilaterally, some advantage will be gained by first pulsing current out of the transistor and then later into the transistor. This follows because, in most PNP transistors, the forward current gain is greater than the reverse current gain which, however, increases with time. It may also be desirable to shape the base current so that the transistor does not become over saturated if one position remains selected.

During the first phase of the turn-off time the base to emitter resistance is very low. In the second phase the base voltage rises to its final value. The external circuitry determines the current flow in the first phase and the ultimate base voltage in the second case. The

optimum driving circuits will be determined from the requirements of the turn-off time and the information derived from measurements on the above phenomenon.

One end of each memory line will be tied to both current sources and the other end will go to individual transistors; thus, the voltage across the memory load of one line will be applied to the outputs of all the non-selected transistors. The base of a non-selected transistor must always be more positive than the collector to emitter voltage so that, for the positive peak load voltage, no load current will flow. Therefore, the maximum load to be driven is determined by the voltage rating of the transistor which must not be exceeded by the sum of the base voltage and the negative peak load voltage.

To maintain the proper current through the selected winding, the reverse currents through the non-selected transistors must be small. As the size of the core memory increases, the added number of reverse current paths creates an increasingly acute problem.

The three important characteristics of the final transistor appear to be:

1. It should have a high current gain at high values of collector current.
2. The recovery time should be short when driving the base with a reasonably low impedance voltage source.
3. The pulses of voltage on the non-selected transistors should not cause appreciable current flow.

There may be other techniques of operation that will allow the transistor more time to recover than the straight forward selection system now used in the memory. If the transistor is returned to the open state as soon as the drive current has stopped, more time would be allowed for reverse recovery. The use of one transistor for READ and one for WRITE would also reduce the recovery requirements. Because the emitter element is smaller than the collector, it is possible that if the two leads, collector and emitter, are interchanged in the above circuit that reverse recovery time would be decreased.

EQUIPMENT NEEDED

The test equipment needs can be fulfilled through the use of Burroughs Unitized Equipment which is available at Lincoln Laboratory. Materials will also be supplied by Lincoln Laboratory

ESTIMATED TIME

Preparation of Proposal	75
Further search of literature	20
Experimental work & analysis	180
Correlation of results and formulation of conclusions	50
Preparation of thesis	75
	400

SIGNED: George A. Davidson
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Date: June 27, 1955

GAD/dg

SUPERVISION AGREEMENT

I consider this material adequate for a Master's Thesis and agree to supervise and evaluate the thesis.

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B-63065

BIBLIOGRAPHY

1. Forrester, J. W., "Digital Information Storage in Three Dimensions Using Magnetic Cores," MIT Servomechanisms Laboratory Report 6R-187, 16 May 1950.

2. Papian, W. N., "A Coincident-Current Magnetic Memory Unit," MIT Servomechanisms Laboratory Report 6R-192, 8 September 1950.

3. Everett, R. R., "Selection Systems for Magnetic Core Storage," MIT Servomechanisms Laboratory Report 6E-413, 7 August 1951.

4. DiNolfo, R. S., "Multi-Coordinate Selection Systems for Magnetic-Core Storage," MIT Lincoln Laboratory Report 6R-235, August 1954.

5. Brown, D. R., "A High-Speed Multiposition Electronic Switch," MIT SM Thesis, May 1947.

6. Gates, E. K., "Transformer Driver for a Coincident Current Magnetic Memory," SM Thesis MIT, 23 August 1954.

7. Canty, W. J., Mitchell, J. L., "Tentative Cathode Estimates for 256 x 256 x 33 and 128 x 128 x 33 Core Memories," MIT Lincoln Laboratory Report 6M-2969, 6 August 1954.

8. Vogelsong, J. H., "A Transistor Pulse Amplifier Using External Regeneration," Proc. IRE, Vol. 41, pp 1444-1450, October 1953.

9. Oken, S., "Transistor Magnetic Core Drivers," SM Thesis, MIT, August 1954.

10. Olsen, K. H., "Transistor Circuits for Driving Coincident-Current Memories," MIT Lincoln Laboratory Report 6M-3316, 21 January 1955.

11. Gray, P., "Pulse-Circuit Characteristics of Power Transistors," SM Thesis, MIT, June 1955.

12. Kingston, R. H., "Switching Time in Junction Diodes and Junction Transistors," Proc. IRE, Vol. 42, pp 829-834, May 1954.

13. Moll, J. L., "Large Signal Transient Response of Junction Transistors," Proc. IRE, Vol. 42, pp 1773-1784, December 1954.

14. Bright, R. L., "Junction Transistors Used as Switches," AIEE Transactions, Vol. 74, part 1, pp 111-121, March 1955.

15. Jones, N. T., "Minority Carrier Storage in Diodes and Transistors," SM Thesis, MIT, August 1954.

16. Brown, D. R., Rochester, N., "Rectifier Networks for Multiposition Switching," Proc. IRE, Vol. 41, pp 1393-1406, October 1953.

17. Webster, W. M., "On the Variation of Junction-Transistor Current-Amplification Factor with Emitter Current," Proc. IRE, Vol. 42, pp 914-920, June 1954.

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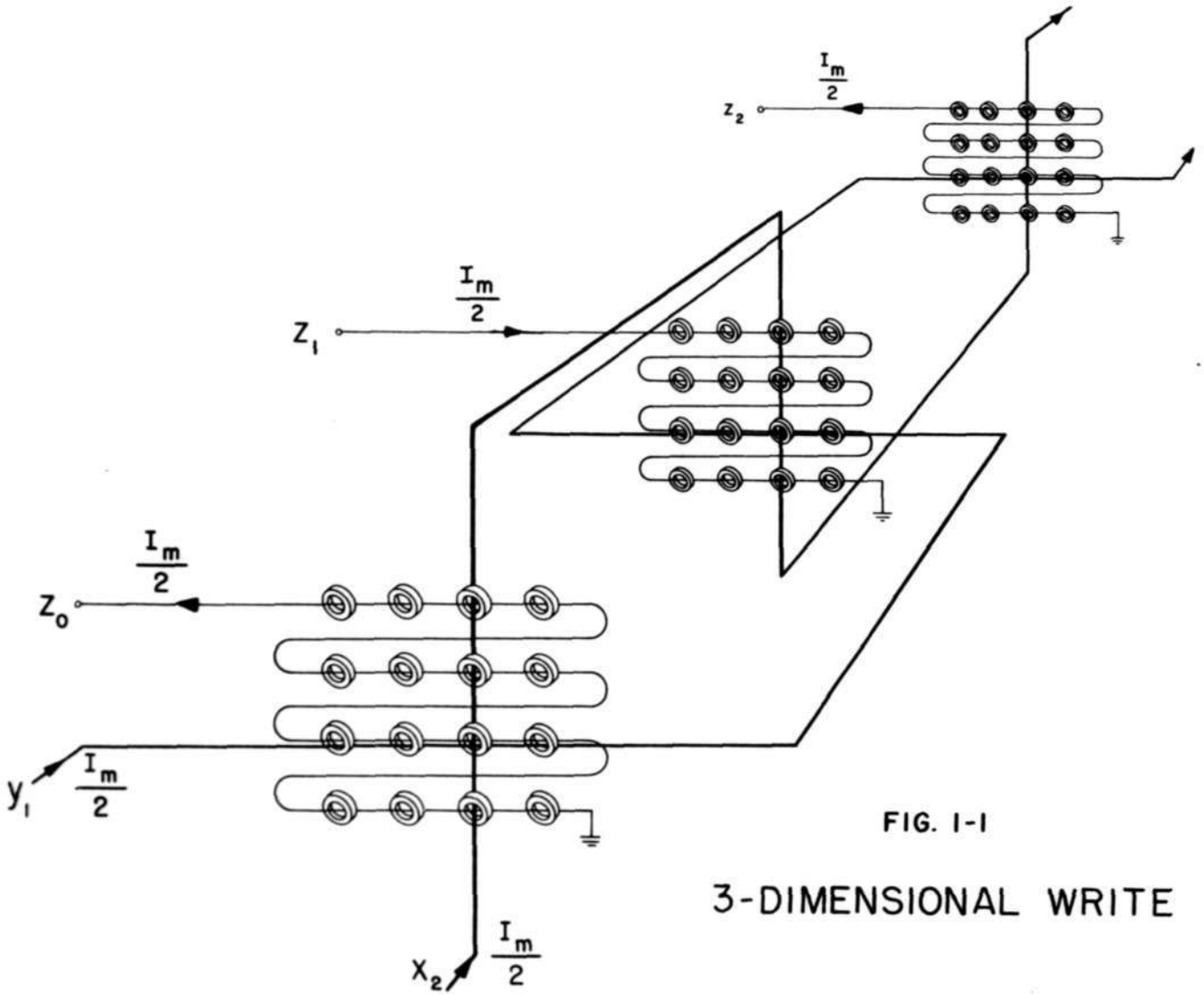

FIG. 1-1

3-DIMENSIONAL WRITE

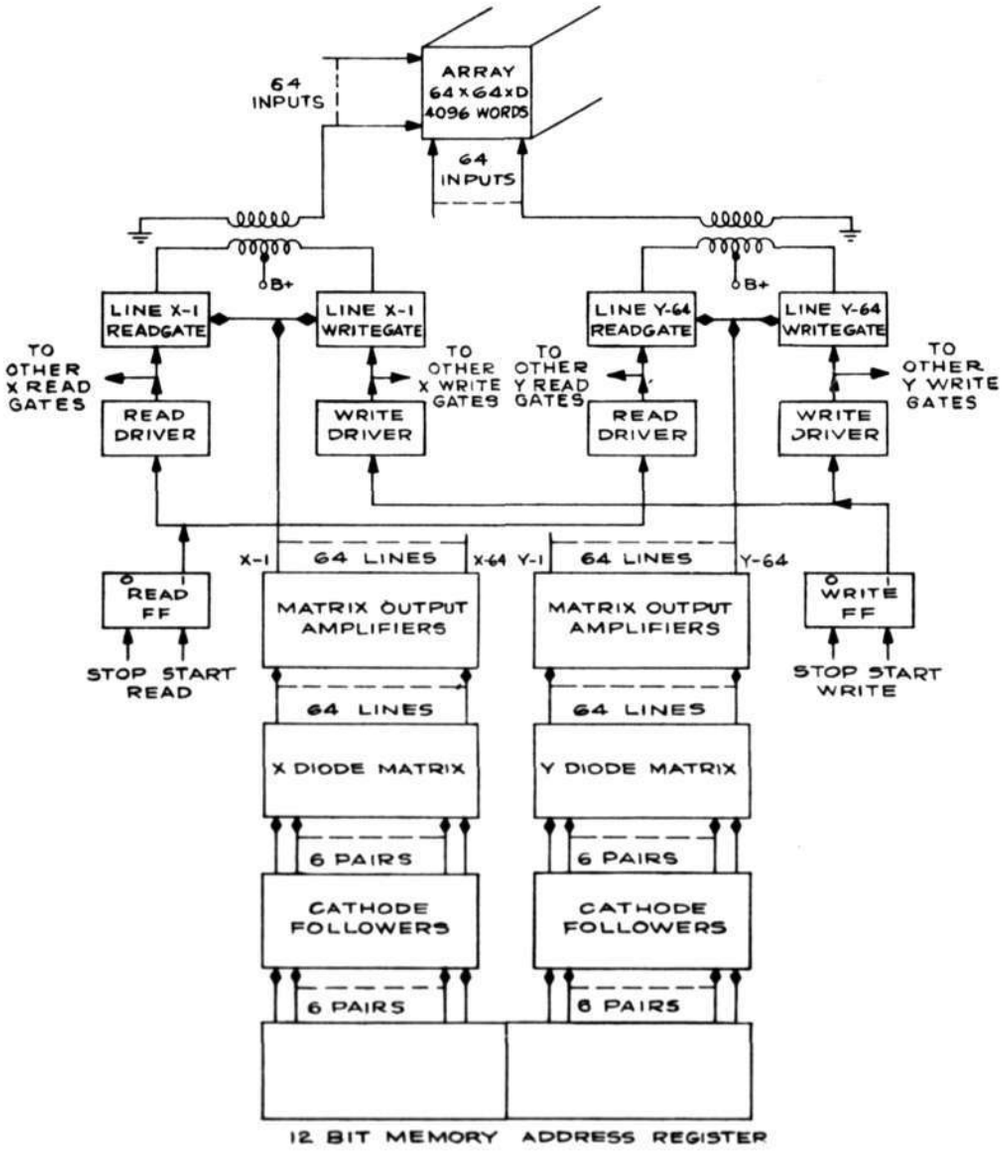

FIG. 1.2
SELECTION SYSTEM BLOCK DIAGRAM

B-6306S